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S.Y. Diploma : Sem. IV [ET/EN/EX/EJ/IE/IS/IC/DE/EV/MU/IU/ED/EI]

Linear Integrated Circuits

Prelim Question Paper Solution

1. (a) (i) 1) Input Offset Current (I_{ios})

The difference between the currents flowing into the inverting and non-inverting terminals of op-amp is called as input offset current I_{ios}.

$$I_{ios} = |I_{B_1} - I_{B_2}|$$

(a) Ideally it is zero, practically it is in nanoamp.

(b) This offset current exists due to mismatch of internal transistor.

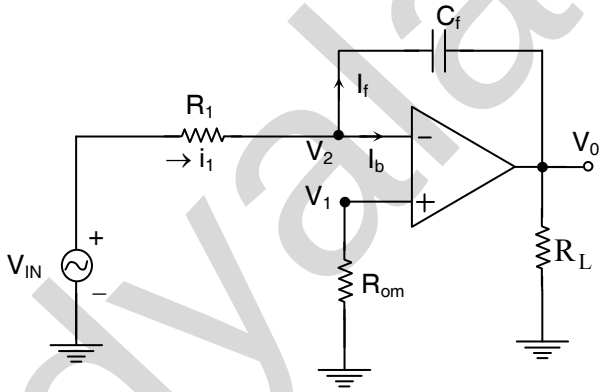
2) CMRR (Common mode Rejection ratio)

It is a ratio of differential open loop gain to the common mode open loop voltage gain.

$$CMRR = \frac{Ad}{Ac}$$

741C – 90 dB

1. (a) (ii) Circuit diagram of basic integrator using op-amp



1. (a) (iii) Specification of IC LM 324

a) Large voltage gain = 100 dB
b) Wide power supply range : 3 V – 32 V
c) Large output voltage swing : 0 V – 32 V
d) Internally frequency compensated for unity gain
e) Input offset voltage : 1.5 mV
f) CMRR : 75 dB

1. (a) (iv) Need of Signal Conditioning

- Signal conditioning means manipulating an analog signal in such a way that it meets the requirements of the next stage for further processing.
- Many physical quantities, Biomedical signals are very weak therefore they need to amplified to sufficiently high level hence conditioning is needed.
- Conditioning is also important is noise rejection.

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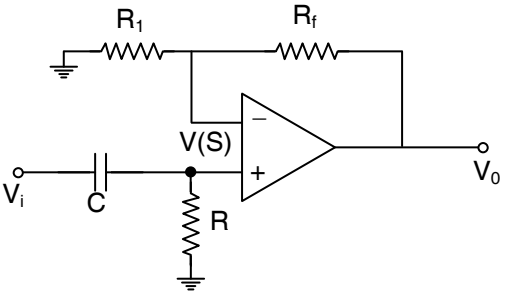
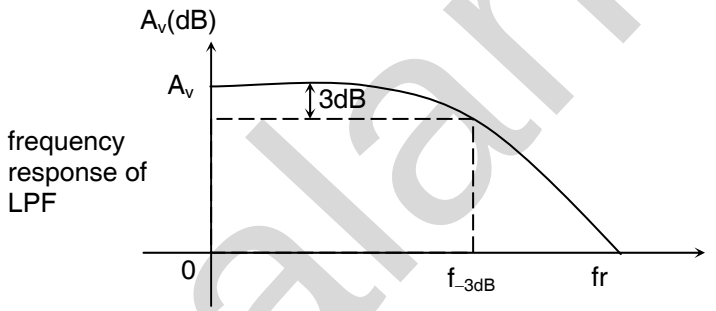
1. (a) (v) 1st order High Pass Filter



1. (a) (vi) 1) Frequency Response

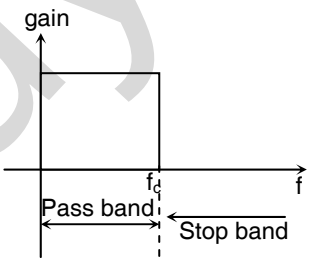
Frequency response of a filter is a graph of gain versus frequency gain is plotted on Y-axis while frequency is plotted on X-axis. The frequency axis is logarithmic axis. So that large frequency range can be plotted in small space gain on Y-axis is in dB.

$dB = 20 \log A_V$



–3 dB Frequency f_{-3dB}/cut-off frequency :

The frequency at which voltage gain is 0.707 i.e., 70.7% of the maximum 0.707 is – 3 dB, it is also defined as frequency at which the power delivered to the load reduces to 50% of it's maximum value.



2) Roll-off rates

The gain falls rapidly in the stop band. The rate at which it falls off is called as the roll off rate.

a) Roll off rate is decided by the order of the filter. If we increase the filter order by 1 then roll off rate is increased by 20 dB/decode.

b) As order of the filter increases frequency response becomes more or more sharp and comes near to the ideal response.

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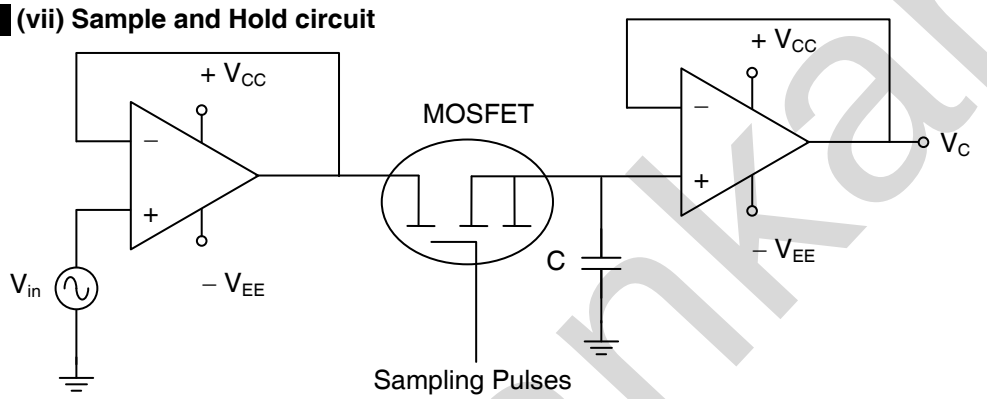
c) Roll off rate of the filter is dependent on the order of the filter i.e., number of poles.
d) One RC network introduces one pole so by increasing number of RC network, number of poles can be increased i.e., order of the filter.
e) Higher order filter offer higher attenuation at frequency beyond the break frequency higher order filters are used when the transition band is to be as narrow as possible.

1. (a) (vii) Sample and Hold circuit



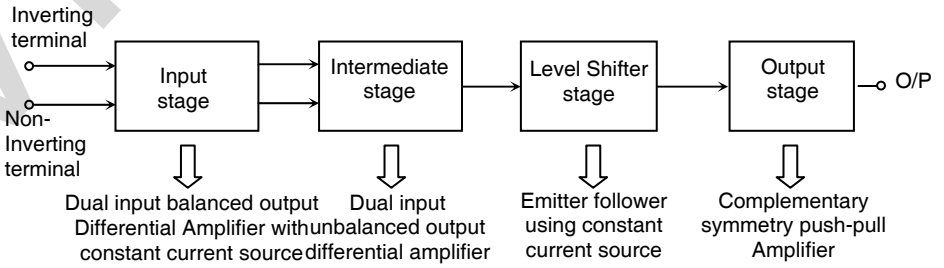
1. (a) (viii) Functions of pins IC 555

1) Trigger

"Trigger": Controls the trigger comparator whose output sets the F/F. For quiscent operation it is connected to $+V_{CC}$, in which case output of trigger comparator is low & $v_0 = 0$. To start the operation, this pin must be brought below 1/3 V_{CC}. As long as voltage at this pin remains below 1/3 V_{CC}, C_2 output remain high. This output goes low when V_2 rises above 1/3 V_{CC}.

2) Control voltage : From internal potential divider, this pin is at $+V_{CC}$ /3. For normal operation a filter C = 0.01μF is connected from this pin to ground. This avoids false triggering due to noise signal. An external voltage connected at this pin changes the reference voltage of both the comparator. This modifies the timing periods and hence this pin can be used for voltage to frequency conversion application.

1. (b) (i) Block diagram of Op-amp



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i) Input stage : This stage provides high voltage gain and high input impedance.
ii) Intermediate stage : This stage provides gain.
iii) Level Shifter stage : As direct coupling is used to couple various input stages in op-amp the dc voltage at the output of intermediate stage is well above ground potential. The level shifter circuit shifts the dc level at the output of the intermediate stage to a pre-determine level.
iv) Output stage : This stage increases the current driving capacity of op-amp.

1. (b) (ii) Parameters of op-amp IC741

Ideal and practical characteristics of op-amp

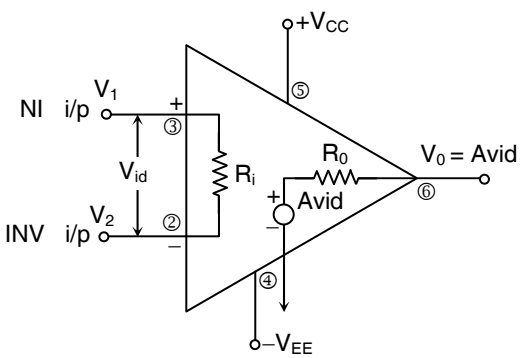
	Characteristics	Ideal	
1.	Input resistance	∞	2 MΩ
2.	Output resistance	0	75Ω
3.	Voltage gain	∞	2×10^5
4.	Bandwidth	∞	$1MH_3$
5.	CMRR	∞	90dB
6.	Slew rate	∞	0.5V/μs
7.	Input offset voltage	0	2mv
8.	PSRR	0	150 μv/v
9.	Input bias current	0	50nA
10.	Input offset current	0	6nA

1. (b) (iii) Equivalent circuit of an op-amp

A_{vid} = equivalent Thevenin voltage source
R_0 = Thevenin equivalent resistance looking back into the output terminal of an op-amp.

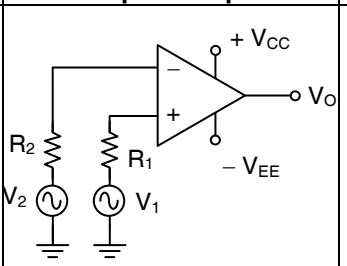
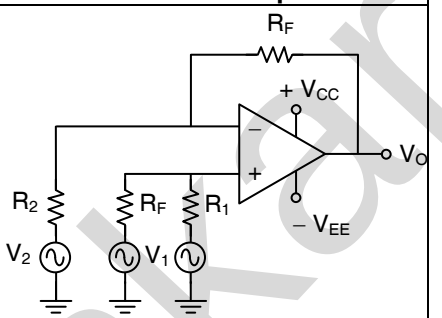
$$V_0 = A_{vid} = A (V_1 - V_2)$$
$$= A (V_{NI} - V_{INV})$$

where A = large signal voltage gain
V_{id} = difference input voltage
V_1 = voltage at non-inverting input terminal w.r.t. ground
V_2 = voltage at inverting input terminal w.r.t. ground



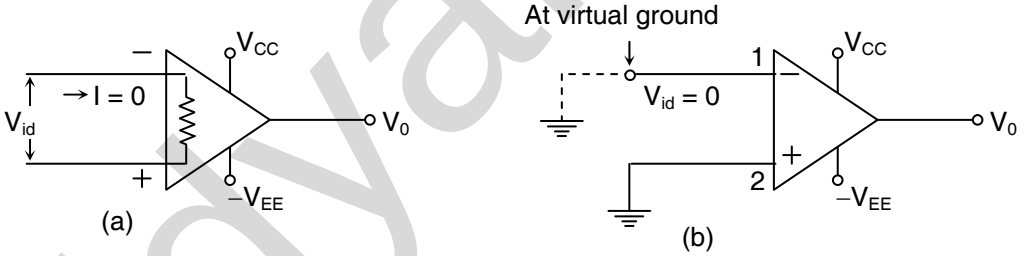
The output voltage is directly proportional to the algebraic difference between the two input voltages, i.e., the op-amp amplifies the difference between two input voltages. It does not amplify the input voltage itself.

2. (a) Compare Open loop and Closed loop configuration

	Parameter	Open Loop	Closed Loop
i)	Circuit		
ii)	Gain	Infinite	Controllable (Depends on R_f and R_2)
iii)	Bandwidth	Less	Bandwidth increases due to negative feedback
iv)	Application	Comparator, Window detector etc.	Adder, Linear amplifier etc.

2. (b) Concept of Virtual Short and Virtual Ground :

While analyzing different op–amp applications two important concepts have to be considered. They are virtual short and virtual ground.



Virtual Short :

According to virtual short concept, the potential difference between two input terminals of an op–amp is almost zero. In other words, both input terminals are approximately at same potential. This concept can be explained as follows.

The input impedance R_i of an ideal op–amp is infinite. So no current flows from one input terminal to other as shown in (a). Thus voltage drop across R_i will be zero and both the input terminals will be at same potential.

Virtual Ground :

In figure (b), the voltage V_{id} = 0 implies that terminal 1 has same potential as terminal 2. Since terminal 2 is grounded, terminal 1 is also virtually grounded. The term "Virtual" is used to imply that since V_{id} = 0, no current flows from terminal 1 to terminal 2. Thus virtual ground point has zero voltage and draws

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no current. The inverting input terminal acts like ground as far as voltage is concerned. So the virtual ground has zero voltage and zero current unlike the usual ground which has zero voltage but can sink infinite current.

In virtual Ground
for closed loop op–amp, we can write

$$V_0 = A.V_{id}$$

i.e. $$A = \frac{V_0}{V_{id}}$$

where A is open loop gain of op–amp and it is very large.

$$\therefore \quad V_{id} = \frac{V_0}{A} \cong 0 = \text{negligibly small}$$

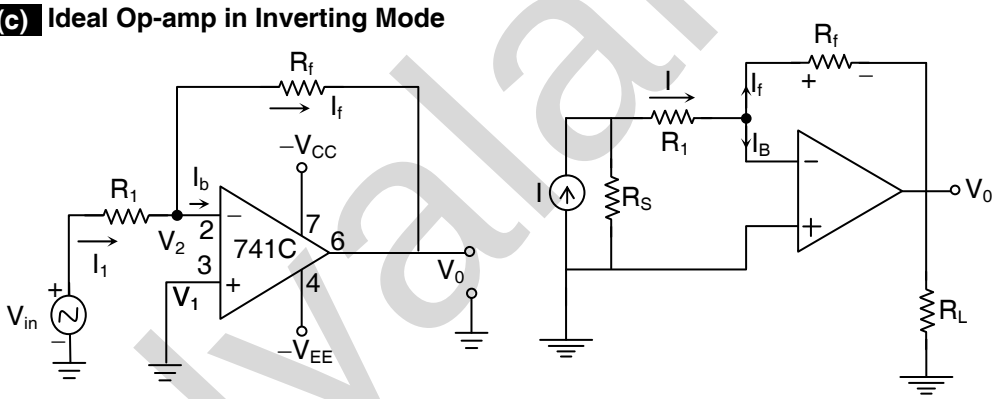
i.e. $V_1 - V_2 = 0$

$\therefore \quad V_1 = 0$

$\therefore \quad V_1 = V_2 = 0$

$\because$ V_1 is at ground potential, V_2 is also virtually at ground potential i.e. for voltage purpose input appears as short circuit and for current purpose it appears as open circuit.

2. (c) Ideal Op-amp in Inverting Mode



The above configuration is a voltage shunt –ve feedback amplifier.
For ideal Op-amp open loop voltage gains ∞.

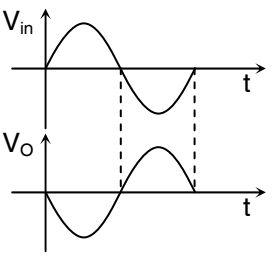
$\therefore \quad A_V = \infty$

Now, $$A_V = \frac{V_O}{V_{id}}$$

$$\therefore \quad V_{id} = \frac{V_O}{\infty} = 0$$

$\therefore \quad V_{id} = V_1 - V_2 = 0$

$\therefore \quad V_1 = V_2$



As shown in the above figure, the non-inverting input terminal is directly connected to ground.

$\therefore \quad V_2 = 0 = V_1$

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i.e., the inverting input terminal is also at ground potential. This is the concept of "virtual ground". Since the current cannot source or sink at this terminal.

For an ideal op-amp, $R_i = \infty$ and $I_B = 0$.
Applying KCL at the negative input terminal,

$I_1 = I_B + I_f$

$\therefore \quad I_1 = I_f \qquad (\because I_B = 0)$

$$\frac{V_{in} - V_2}{R_1} = \frac{V_2 - V_0}{R_f}$$

But $V_2 = 0V$ …… by concept of virtual ground.

$$\therefore \quad \frac{V_{in}}{R_1} = -\frac{V_0}{R_f}$$

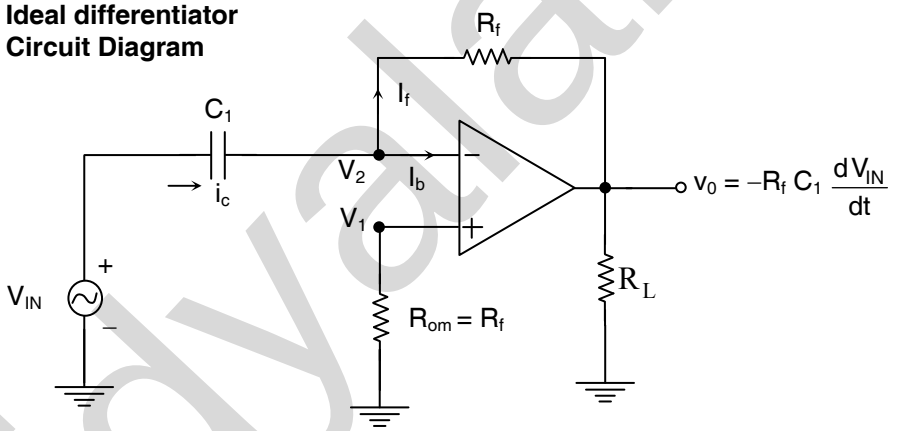
$$\therefore \quad \frac{V_0}{V_{in}} = -\frac{R_f}{R_1} = A_{fb} \text{ (Gain with feedback)}$$

$$\therefore \quad V_0 = -\frac{R_f}{R_1} V_{in}$$

The –ve sign indicates that the output voltage is 180° out of phase w.r.t. the input voltage.

2. (d) Ideal differentiator

Circuit Diagram



The circuit diagram in which the output waveform is the derivative of the input waveform, is known as a differentiator. It can be constructed from a basic inverting amplifier by just replacing input resistor R_1 by a capacitor C_1. For ideal amp. $R_i = \infty$ hence $I_B \approx 0$. Similarly $A_v = \infty$

$$\therefore \quad v_{id} = \frac{v_C}{Av} = 0$$

$\therefore \quad V_1 - V_2 = 0$

$\therefore \quad V_1 = V_2$

But $V_1 = 0$ hence $V_2 = 0$ which is the virtual ground concept. Also in any capacitor $q = Cv$

$$\therefore \quad \frac{dq}{dt} = i_C = C\frac{dv_C}{dt}.$$

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Now applying KCL at the inverting input terminal, $i_C = I_B + i_f$ since $I_B \cong 0$

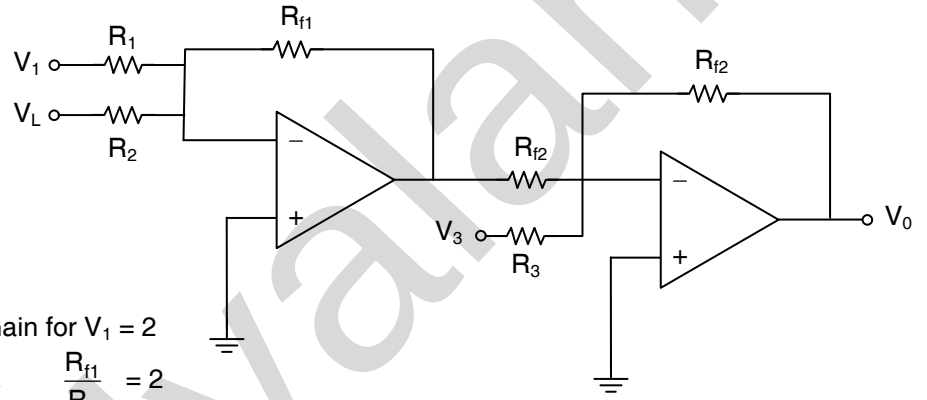
$\therefore \quad i_C = i_f$ i.e. $C_1 \frac{d}{dt}(v_{in} - V_2) = \frac{v_2 - v_0}{R_f}$.

But $v_2 = 0$

$\therefore \quad C_1 \frac{dv_{in}}{dt} = -\frac{v_0}{R_f} \quad \therefore V_0 = -R_f C_1 \frac{dv_{in}}{dt}$

Thus the output voltage v_0 is equal to $R_f C_1$ times the negative instantaneous rate of change of input voltage v_{IN} with time. Since differentiator performs the opposite operation of integrator, a cosine input will produce a sine wave output or a triangular input will produce a square wave output. For a square wave input, the circuit will produce positive going and negative going pulses, provided, the time constant $R_f C_1 < < T$ where T is the periodic time of the input waveform. The above circuit has some drawbacks which are eliminated in a practical differentiator.

2. (e) $V_0 = 2V_1 + V_2 - 5V_3$



Gain for $V_1 = 2$

$\therefore \quad \frac{R_{f1}}{R_1} = 2$

$R_{f1} = 2R_1$

Let $R_1 = 1\ k\Omega$

$R_{f1} = 2\ k\Omega$

Gain for $V_2 = 1$

$\frac{R_{f1}}{R_L} = 1$

$R_{f1} = R_L$

$\therefore \quad R_2 = 2k\Omega$

Gain for $V_3 = \frac{R_{f2}}{R_3}$

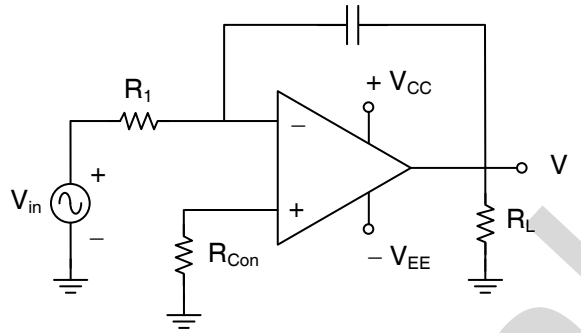
$5 = \frac{R_{f2}}{R_3}$

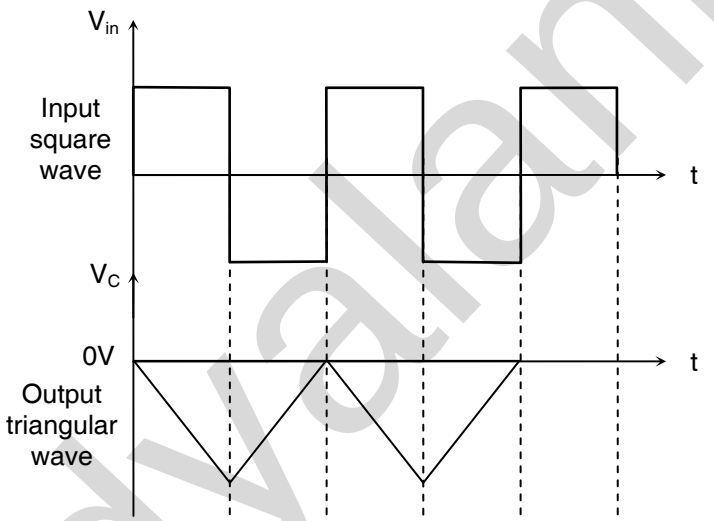
$R_{f2} = 5\ R_3$

Let $R_3 = 1.5\ k\Omega$
$R_{f2} = 5 \times 1.5\ k\Omega$
$R_{f2} = 7.5\ k\Omega$

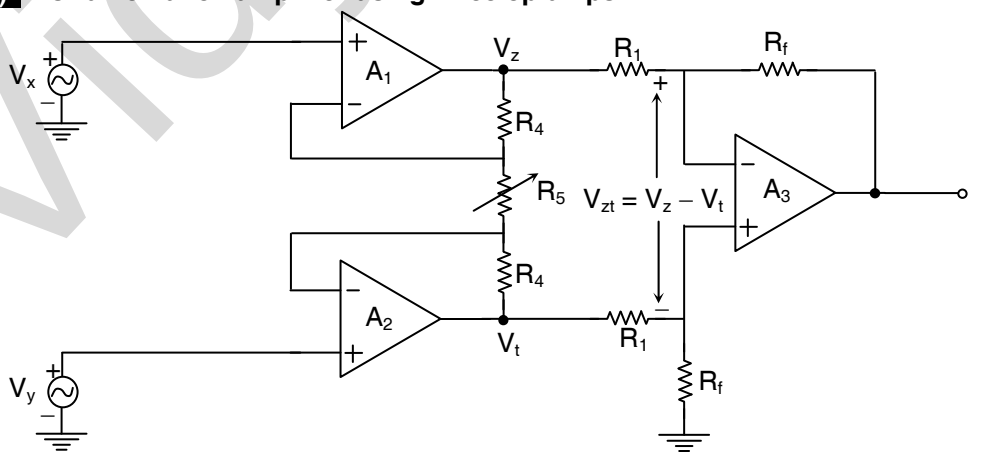
2. (f) Op-amp based circuit

An Integrator circuit can convert square wave into triangular waveform.





3. (a) Instrumentation amplifier using three op-amps



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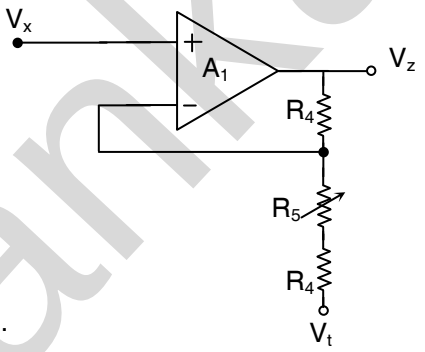
A_1, A_2, A_3 μA725 High slew rate Op–Amp.

$$v_0 = \left(1+\frac{2R_4}{R_5}\right)\left(\frac{R_f}{R_1}\right)\left(V_y - V_x\right)$$

The instrumentation amp. using 3 Op–Amps which is most popular is shown in the figure. For good performance, high slew rate Op–Amp. μA 725 are used. The Op–Amps A_1 and A_2 are used in Non–inverting mode to which 2 signals V_x and V_y are given as input. The input stage provides very high R_i because of non-inverting mode. The Op–Amp A_3 is used as a difference amplifier, providing additional gain. The gain of the entire circuit is controlled by varying only 1 potentiometer R_5. Basically the circuit amplifies the difference 2 input signals A_x & A_y.

Derivation of A_v :

Circuit for Op–Amp. A_1 is re–drawn. It has 2 input signals V_x and V_t with V_z as output. To find V_z use super – position theorem. Let V_x be the only input present while V_t is grounded A_1 is now in Non–inverting mode & its gain is $\left(1+\frac{R_f}{R_1}\right)$ where $R_f = R_4$ and $R_1 = R_4 + R_5$.



Hence gain $A_{fb} = \left(1+\frac{R_4}{R_4+R_5}\right) = \left(\frac{2R_4+R_5}{R_4+R_5}\right)$.

Hence the output V_z' due to only V_x is given by

$$V_z' = \left(\frac{2R_4+R_5}{R_4+R_5}\right)V_z.$$

Now put V_x = 0 & let V_t be the only input signal. The gain of this inverting mode op–amp. is

$-\frac{R_f}{R_1}$. i.e. $A_{fb} = -\frac{R_4}{R_4+R_5}$. Hence $V_z'' = \left(\frac{-R_4}{R_4+R_5}\right)V_t$.

By superposition, $V_z = V_z' + V_z'' = \left(\frac{2R_4+R_5}{R_4+R_5}\right)V_x - \left(\frac{R_4}{R_4+R_5}\right)V_t$ … (i)

Similarly considering Op–Amp. A_2 done, the 2 input signals are V_y (Non–inverting mode) and V_z (inverting mode) and its output is V_t. Applying super–position theorem exactly same way, we get

$$V_t = V_t' + V_t'' = \left(\frac{2R_4+R_5}{R_4+R_5}\right)V_y - \left(\frac{R_4}{R_4+R_5}\right)V_z \quad \text{… (ii)}$$

The Op–Amp A_3 is working as Difference amplifier and input to A_3 is given by $V_{zt} = V_z - V_t$.

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Putting the values from equations (i) & (ii) we get

$$(V_z - V_t) = \left(\frac{2R_4 + R_5}{R_4 + R_5}\right)V_x - \left(\frac{R_4}{R_4 + R_5}\right)V_t - \left(\frac{2R_4 + R_5}{R_4 + R_5}\right)V_y + \left(\frac{R_4}{R_4 + R_5}\right)V_z$$

$$= \left(\frac{2R_4 + R_5}{R_4 + R_5}\right)(V_x - V_y) + \left(\frac{R_4}{R_4 + R_5}\right)(V_z - V_t)$$

$$\therefore \quad (V_z - V_t)\left\{1 - \frac{R_4}{R_4 + R_5}\right\} = \frac{(2R_4 + R_5)}{(R_4 + R_5)}(V_x - V_y)$$

$$\therefore \quad (V_z - V_t)\left\{\frac{R_4 + R_5 - R_4}{(R_4 + R_5)}\right\} = \frac{(2R_4 + R_5)}{(R_4 + R_5)}(V_x - V_y)$$

$$\therefore \quad (V_z - V_t) = \left(\frac{2R_4 + R_5}{R_5}\right)(V_x - V_y)$$

This is the input signal to the Difference amp. A_3 whose gain is given by $\left(-\frac{R_f}{R_1}\right)$.

The –ve sign comes since V_{zt} is assumed to be +ve at inverting input of A_3. Hence the final output is given by

$$v_0 = \left(\frac{2R_4 + R_5}{R_5}\right)(V_x - V_y) \times \left(-\frac{R_f}{R_1}\right)$$

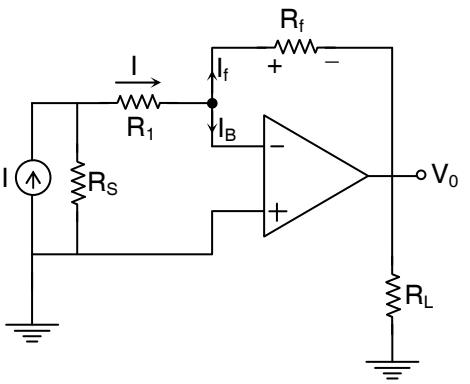
$$\therefore \quad v_0 = \left(\frac{R_f}{R_1}\right)\left(\frac{2R_4 + R_5}{R_5}\right)(V_y - V_x)$$

$\therefore$ Total voltage gain of the system is given by $\frac{v_0}{(V_y - V_x)} = \left(\frac{R_f}{R_1}\right)\left(\frac{2R_4 + R_5}{R_5}\right)$. Thus the gain can be controlled by varying potentiometer R_5 alone since all other resistors are fixed.

Only $R_5 \neq 0$. Since the gain is not defined. Also if $R_5 = \infty$ i.e. open circuit, then A_1 and A_2 operate as voltage follower & no voltage gain is possible by the first stage.

3. (b) Current to Voltage Converter

I to V converter is nothing but a special case of inverting amplifier. As shown in the diagram input voltage signal is replaced by a constant current source. For ideal Op–Amp, $R_i = \infty$ hence $I_B \approx 0$. Similarly $A_V = \infty \therefore v_{id} = V_1 - V_2 = 0 \therefore V_1 = V_2$. Due to virtual ground concept, $V_2 = 0$.



Applying KCL at inverting input,

$$I = I_B + I_f = I_f \qquad [\because I_B \approx 0]$$

Now $\quad I_f = \frac{V_2 - V_0}{R_f} = -\frac{V_0}{R_f} \quad [\because V_2 = 0]$

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Hence $I = -\frac{V_0}{R_f}$

$\therefore \quad V_0 = -IR_f$.

Thus $v_0 \propto I$ and hence the input current is converted into corresponding output voltage and the circuit works as a current to voltage converter.

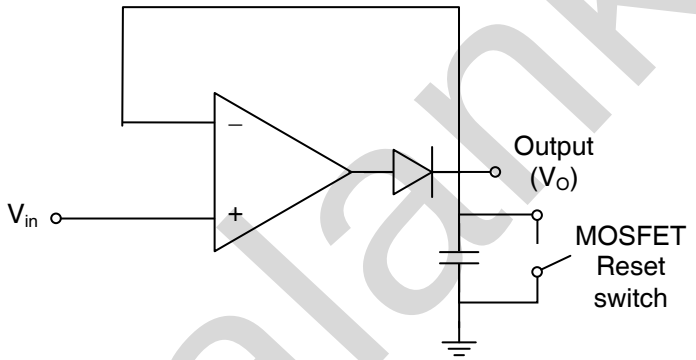
Applications

(i) The most common use is in Digital to Analog converter i.e. in binary or R–2R ladder N/W.

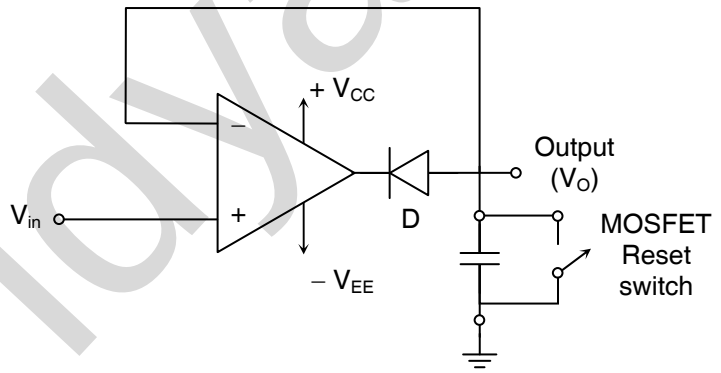
(ii) Used for sensing current through photodetectors such as photo–cells, photo–diodes and photovoltaic cells.

3. (c) Circuit diagram of Peak detector (Positive Peak and Negative Peak)

Positive Peak Detector



Negative Peak Detector



3. (d) Analog Multiplier

There are a number of applications of analog multiplier such as frequency doubling, frequency shifting, phase angle detection, real power computation, multiplying two signals, dividing and squaring of signals. A basic multiplier schematic symbol is shown in figure. Two signal inputs (v_x and v_y) are provided. The output is the product of the two inputs divided by a reference voltage V_{ref}.

$$V_0 = \frac{v_x y_y}{V_{ref}} \qquad \ldots (A)$$

Normally, V_{ref} is internally set to 10 volt.

So, $V_0 = \frac{v_x y_y}{10}$

As long as $v_x < V_{ref}$
and $v_y < V_{ref}$
the output of the multiplier will not saturate.

If both inputs are positive, the IC is said to be a one quadrant multiplier. A two quadrant multiplier will function properly if one input is held positive and the other is allowed to swing both positive and negative. If both inputs may be either positive or negative, the IC is called a four quadrant multiplier.

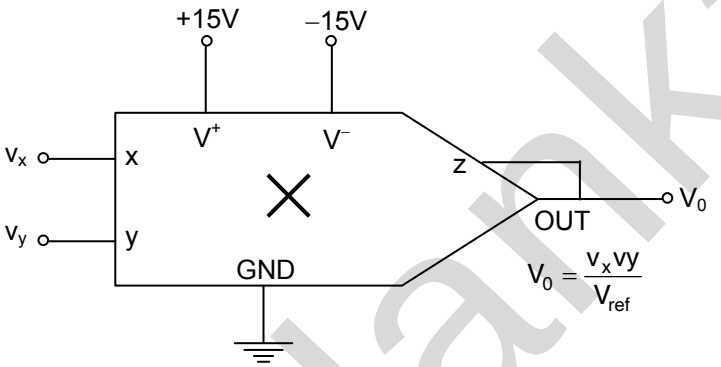


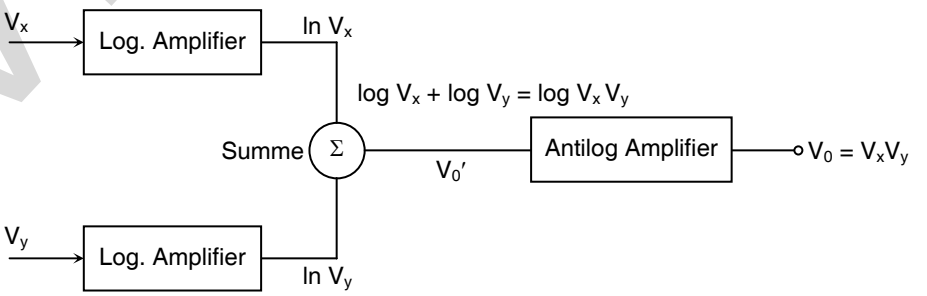
Fig. : Multiplier schematic symbol

There can be several ways to make a circuit which will multiply according to equation (A). One commonly used technique is log–antilog method. The log–antilog method relies on the mathematical relationship that the sum of the logarithm of two numbers equals the logarithm of the product of those numbers.

$$\ln V_x + \ln V_y = \ln(V_x V_y)$$

Figure below is a block diagram of a log-antilog multiplier IC. Log–amps require the input and reference voltages to be of the same polarity. This restricts log–antilog multipliers to one quadrant operation. A technique that provides four quadrant multiplication is transconductance multiplier. Some of the multiplier IC chips available are AD533 and AD534.

The multiplier operation can be performed using log and antilog amplifier:



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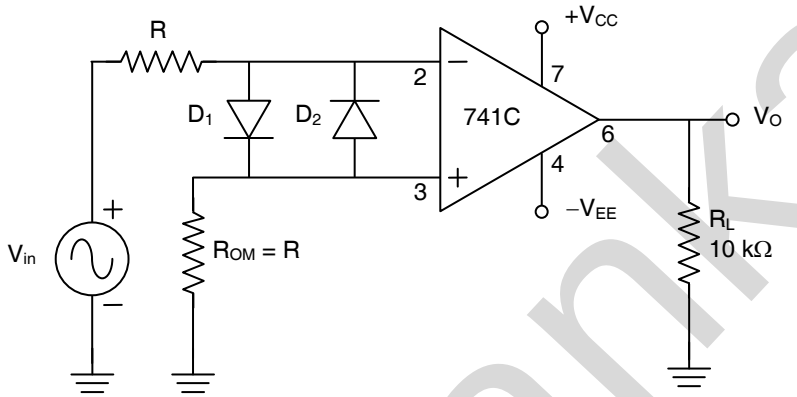
$$V_0' = \ln V_x + \ln V_y$$

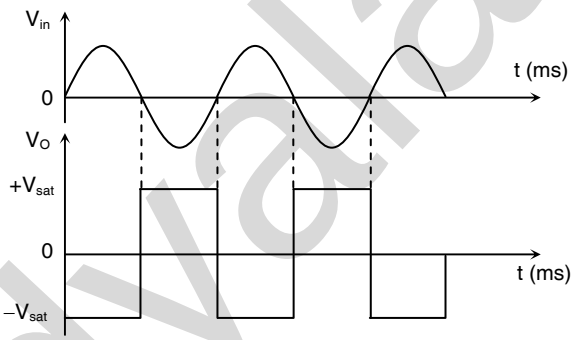
$$V_0' = \ln V_x V_y$$

$$V_0 = \ln . \ln^{-1} V_x V_y$$

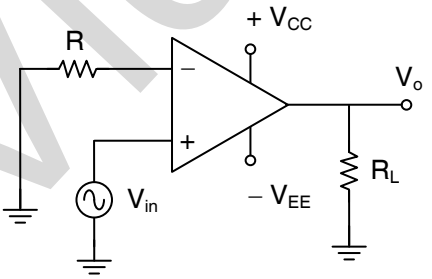
$V_0 = V_x V_y$ Hence output is multiplication or product of V_x and V_y.

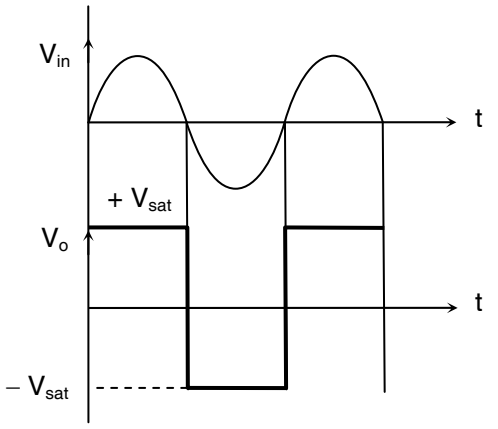
3. (e) Inverting Zero Crossing Detector





Non-Inverting ZCD





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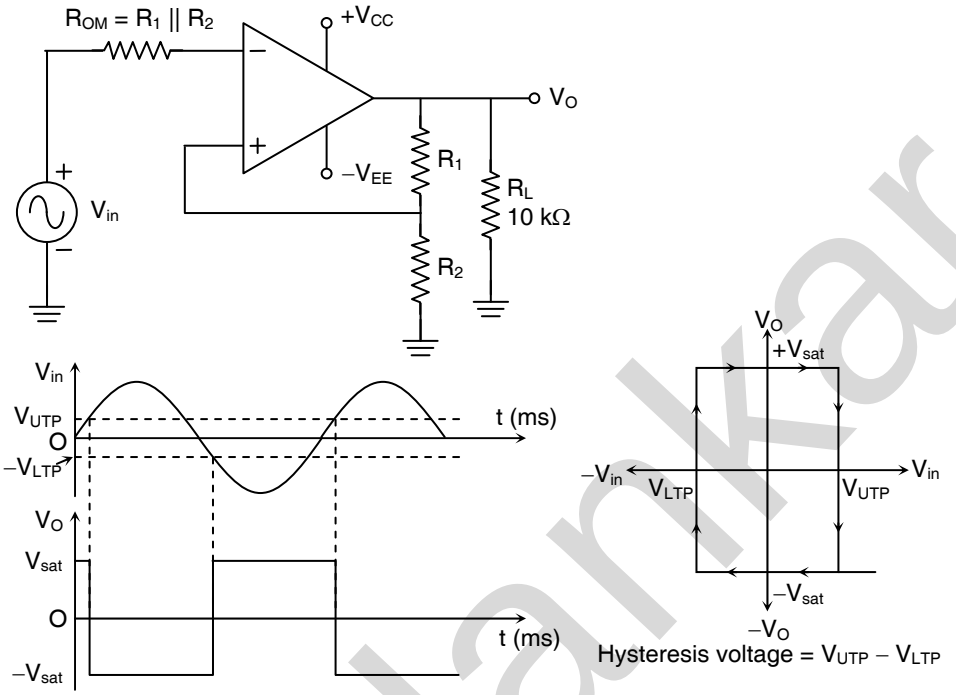
3. (f) Schmitt Trigger



The figure shows an inverting comparator with positive feedback. This circuit converts an irregular shaped waveforms to a square wave or pulse. The circuit is known as Schmitt Trigger or squaring circuit.

As shown in the figure above, by using a potential divider circuit, R_1 and R_2, some portion of V_O is feedback at the +ve (Non-inverting) input terminal. This constitutes positive or regenerative feedback.

The input voltage V_{in} triggers (changes the state of) the output V_O everytime it exceeds certain voltage levels called upper threshold point (V_{UTP}) and lower threshold point (V_{LTP}). These threshold voltages are obtained by using the voltage divider R_1 and R_2. The voltage across R_1 is feedback to the non-inverting input terminal.
The voltage across R_1 is a variable reference threshold voltage which depends on the value and polarity of the output voltage V_O.

When $V_O = +V_{sat}$, the voltage across R_1 is called the upper threshold voltage, V_{ut}. The input voltage V_{in} must be slightly more positive than V_{ut} in order to cause the output voltage V_O to switch from $+V_{sat}$ to $-V_{sat}$.

As long as $V_{in} < V_{ut}$, $V_O = +V_{sat}$

$$\therefore \quad V_{ut} = \frac{R_1}{R_1 + R_2} (+V_{sat})$$

Now V_{in} starts increasing and when $V_{in} = V_{ut}$, V_O is driven to $= -V_{sat}$.

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Now, when $V_O = -V_{sat}$, voltage across R_1 is referred to as lower threshold voltage V_{lt}. V_{in} must be slightly more –ve than V_{lt} in order to cause V_O to switch from $-V_{sat}$ to $+V_{sat}$.

$$\therefore \quad V_{lt} = \frac{R_1}{R_1 + R_2}(-V_{sat})$$

- If threshold voltages V_{ut} and V_{lt} are made larger than the input noise voltages, the +ve feedback will eliminate the false output transitions.
- Positive feedback because of its regenerative action, will make V_O switch faster between $+V_{sat}$ and $-V_{sat}$.
- $R_{OM} \cong R_1 \parallel R_2$ is used to minimize the offset problem.

The comparator with positive feedback is said to exhibit hysteresis, a deadband condition

i.e., when V_{in} exceeds V_{ut}, the output switches from $+V_{sat}$ to $-V_{sat}$ and reverts back to $+V_{sat}$, when the input goes below V_{lt}.

The hysteresis voltage is given as

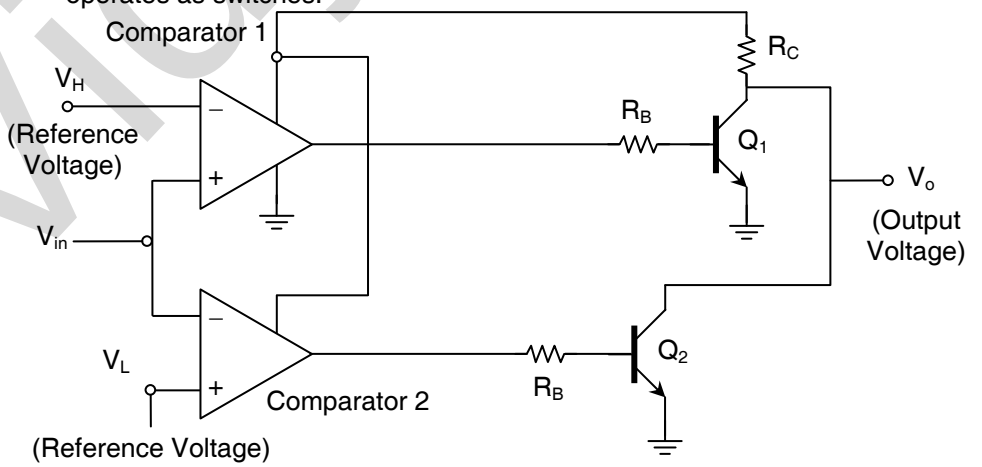
$$V_{hy} = V_{ut} - V_{lt}$$

$$= \frac{R_1}{R_1 + R_2}[(+V_{sat}) - (-V_{sat})]$$

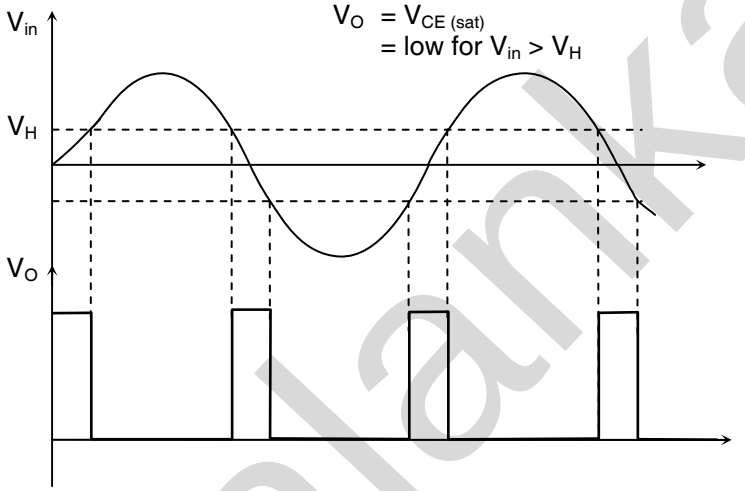
(i) It is used a sine to square wave converter.
(ii) Any irregular shaped waveform is converted into square wave.
(iii) It is used in analog to digital converter since analog voltage gets converted into digital voltage.
(iv) It is used as an amplitude comparator, to know the instance at which V_{in} attains a particular voltage level. This is done by comparing it with UTP and LTP.
(v) Since it has two stable states, it can be used as a flip-flop.

4. (a) Window Detector

- The window detector circuit is used for detecting whether an unknown voltage V_{in} falls within a specified voltage band called window.
- V_H and V_L are two reference voltages with $V_H > V_L$ and V_{in} the input voltage. The outputs of the two comparators are applied to two transistors which operates as switches.



- If V_{in} is between the two reference voltages i.e. $V_L < V_{in} < V_H$ then the outputs of both the comparators will be low. So both the transistors will remain in off state. So the collector voltage i.e. $V_o = + V_{CC}$ for $V_L < V_{in} < V_H$.
- If V_{in} is less than V_L then the output of comparator 1 will be low and that of comparator 2 will be high. This will turn off transistor Q_1 but staturate transistor Q_2 and output voltage will be $V_{CE(sat)}$ i.e. low.
  $V_o = V_{CE\ (sat)}$ = Low for $V_{in} < V_L$
- If V_{in} is greater than V_H then the of comparator 1 will be high and that of comparator 2 will be low. Thus transistor Q_1 will saturate and Q_2 will remain off. The output voltage will be $V_{CE\ (sat)}$ i.e. low.



4. (b) $\because$ $f_L = 1$ KHz

$\because$ $f_L = \dfrac{1}{2\pi RC}$

Let $C = 0.01\ \mu F$

$\therefore$ $R = \dfrac{1}{2\pi f_L C}$

$R = \dfrac{1}{2\pi \times 1KHz \times 0.01\mu}$

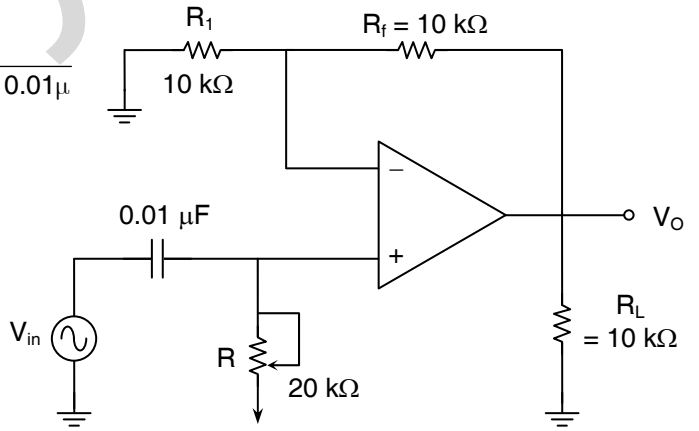
$R = 15.9\ k\Omega$

$\because$ $A_F = 1 + \dfrac{R_F}{R_1}$

$Z = 1 + \dfrac{R_F}{R_1}$

$R_F = R_1$

Let $R_1 = R_f = 10\ k\Omega$



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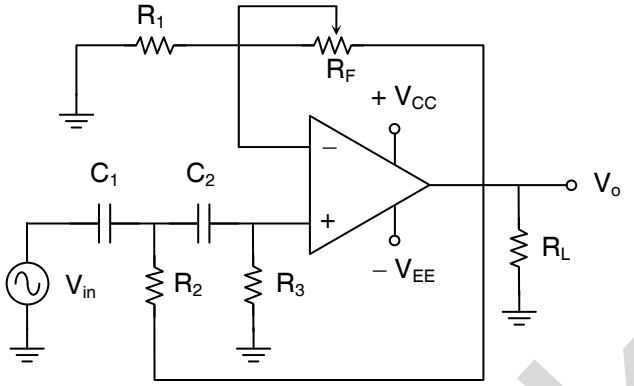
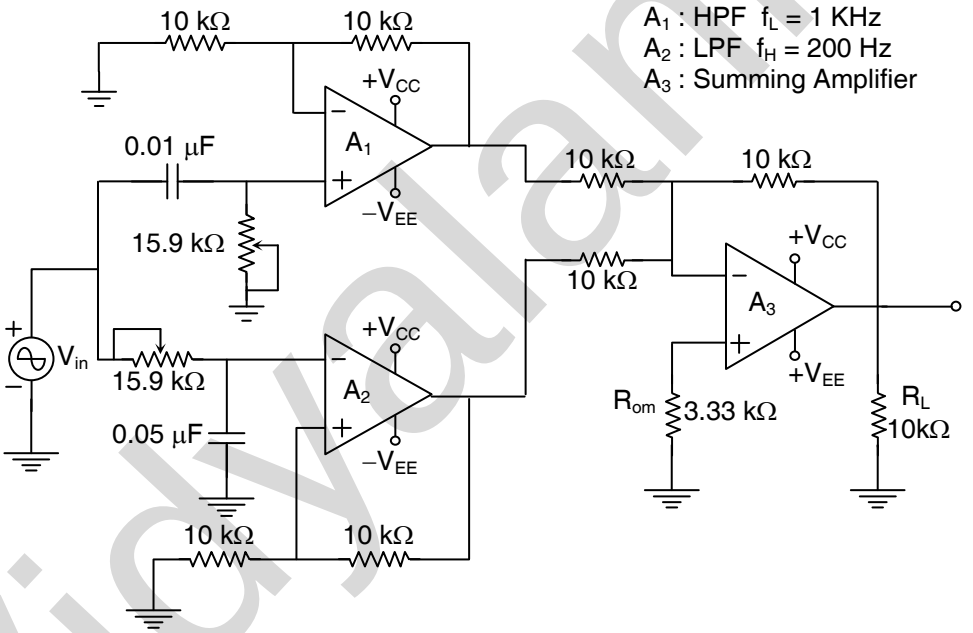
4. (c) Op-amp based circuit using Butterworth filter to fulfill response

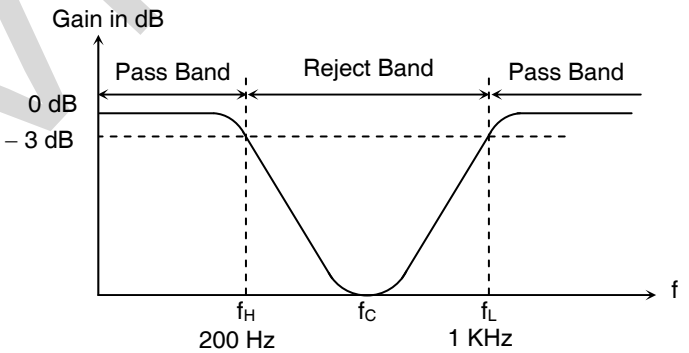


4. (d) Broad Band Reject Filter

(a) Circuit Diagram



(b) Frequency Response



$$f_C = \sqrt{f_H \times f_L}$$

$$= 447.2 \text{ Hz}$$

$$Q = \frac{f_C}{B.W.} = \frac{f_C}{f_L - f_H}$$

$$= \frac{447.2}{800}$$

$$= 0.56 < 10$$

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Band stop (elimination or reject) filters are also classified into 2 groups (i) Broad band if Q < 10, (ii) Narrow band if Q > 10. As the name suggests if Q > 10 then the stop band of the filter is very narrow. As shown in the circuit diagram, wide band reject filter can be constructed by using L. P. F. , H. P. F. and a summing amplifier. To realize the band–reject frequency response the cut–off frequency f_L of H. P. F. must be greater than the cut–off frequency f_H of L. P. F. In addition, the gain of both H. P. F. and L. P. F. must be equal and their orders must be same. As shown in the frequency characteristics, for $f < f_H$, the signal is rejected by H. P. F. but since $f_H < f_L$, it is allowed to pass by L. P. F. On the other hand if $f > f_L$ then H. P. F. allows the signal to pass to the summing amplifier. Thus if $f < f_H$ or $f > f_L$, the signal is passed to the output without any attenuation. On the other hand if $f_H < f < f_L$ then the signal is rejected by the filter. For this filter also, the following relations hold true.

(i) $f_C = \sqrt{f_H \times f_L}$ (ii) $Q = \dfrac{f_C}{B.W.}$

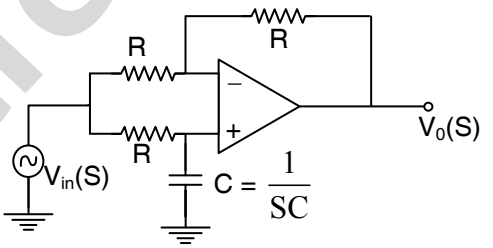
For the circuit shown above, $f_H = 200Hz$, $f_L = 1000Hz$

$\therefore \quad f_C = 447.2$ & $Q = \dfrac{447.2}{800} = 0.56.$

Since Q < 10, this is a broad band reject filter. For better performance a R_{OM} of 3.3k (10k// 10k // 10 k) is connected to positive input terminal of summing amplifier. This R_{OM} acts as a compensation resistor for offset voltage.

4. (e) All Pass Filter

As the name suggests, an all pass filter passes all frequencies without attenuation by providing predictable phase shift for different frequencies of input signal.



Analysis : Using superposition theorem to analyse the above circuit we get,

$$V_0(S) = V_{0_1}(S) + V_{0_2}(S)$$

$V_{0_1}(S)$ is output due to input at inverting terminal.

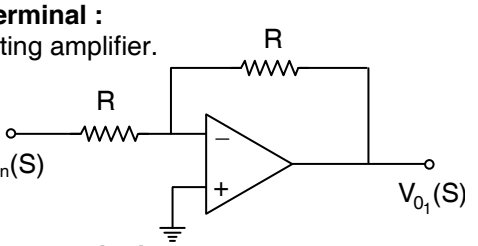
$V_{0_2}(S)$ is output due to input at non-inverting terminal.

(i) Considering only input to inverting terminal :

The circuit shown in figure acts as inverting amplifier.

$$V_{0_1}(S) = -\frac{R_f}{R_1} V_{in}(S) = -\frac{R}{R} V_{in}(S)$$

$$V_{0_1}(S) = -V_{in}(S) \qquad \ldots (1)$$



(ii) Considering only input to non-inverting terminal :

The circuit shown in figure acts as non-inverting amplifier.

$$V_{0_2}(S) = (1+\frac{R_f}{R_1})\, V_1(S) \qquad = (1+\frac{R}{R})\, V_1(S)$$

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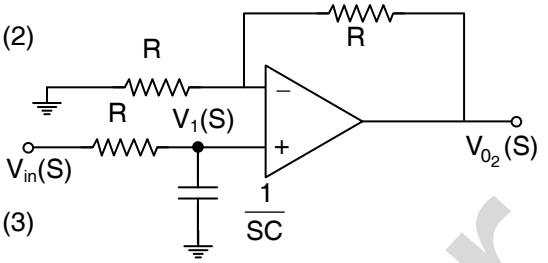
$$V_{0_2}(S) = 2V_1(S) \quad \ldots (2)$$

$$V_1(S) = \frac{1/SC}{R+\frac{1}{SC}} V_{in}(S)$$

$$V_1(S) = \frac{1}{1+RSC} V_{in}(S) \quad \ldots (3)$$



Putting equation (3) in equation (2)

$$V_{0_2}(S) = \frac{2}{1+RSC} V_{in}(S)$$

Putting $V_{0_1}(S)$ and $V_{0_2}(S)$ in V_0.

$$V_0(S) = -V_{in}(S) + \frac{2}{1+SRC} V_{in}(S) = V_{in}(S)\left[\frac{2}{1+SCR} - 1\right]$$

$$= V_{in}(S)\left[\frac{1-SCR}{1+SCR}\right]$$

$$\frac{V_0(S)}{V_{in}(S)} = \left[\frac{1-SCR}{1+SCR}\right]$$

$$A_v(S) = \left[\frac{1-SCR}{1+SCR}\right]$$

$$A_v(jw) = \left[\frac{1-jwCR}{1+jwCR}\right]$$

$$Av(j2\pi f) = \frac{1-j2\pi FCR}{1+j2\pi FCR}$$

$$A_v(jf) = \frac{1-j(f/f_1)}{1+jf/f_1} \qquad \text{where } f_1 = \frac{1}{2\pi RC}$$

$$|A_v(f)| = \frac{\sqrt{1+(f/f_1)^2}}{\sqrt{1+(f/f_1)^2}}$$

$$|A_v(f)| = 1 \quad \ldots (4)$$

$$\phi = \frac{\tan^{-1}(-f/f_1)}{\tan^{-1}(f/f_1)} = \tan^{-1}(-f/f_1) - \tan^{-1}(f/f_1)$$

$$= -2\tan^{-1}\frac{f}{f_1} \quad \ldots (5)$$

It is seen from above equation that amplitude of the amplifier or gain of amplifier to all the frequencies remain the same and phase shift between V_0 and V_{in} is function of frequency.

Application

When signals are transmitted over transmission on lines, such as Telephone wires they undergo phase shift or change in phase. To compensate for this phase changes all pass filter are used.

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4. (f) Classification of Op-amp filters

1) Components used

- Active filter
- Passive filter

2) Frequency Range

- Audio frequency
- Radio frequency

3) Frequency Response

- Low pass filter
- High pass filter
- Band pass filter

4) Nature of pass band and stop

Pass band

- Wide band pass filter
- Narrow band pass filter

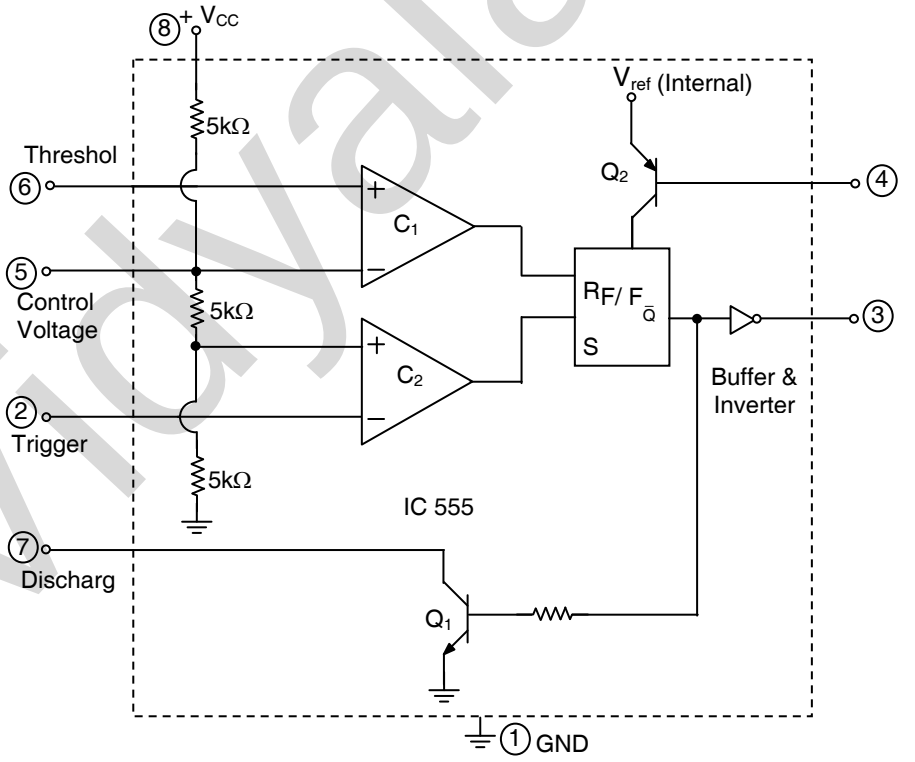
Stop band

- Wide band stop filter
- Narrow band stop filter

5. (a) Block diagram of IC 555

Timer IC 555

Functional diagram



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The important internal block of the I.C. are

(i) 2 No. of comparators :
  (a) Thresh–hold comparator C_1,
  (b) Trigger comparator C_2.
(ii) R–S F/F
(iii) Buffer cum inverter
(iv) 2 Transistors : (a) Discharge transistor Q_1, (b) Reset Transistor Q_2.
(v) Potential divider formed by 3 equal value 5kΩ resistors.

Operation

When the supply is given, the output depends upon the voltages at pin no.2 (trigger) and 6 (thresh–hold). If $V_2 > 1/3\ V_{CC}$ and $V_6 < \frac{2V_{CC}}{3}$ are satisfied at the start, the output of C_1 and C_2 are low, the F/F is reset. The output $v_0 = 0$ and the circuit is in quiscent state. The internal Transistor Q_1 is in saturation which clamps the pin 7 (discharge) to the ground potential. This prevents C_{EXT}. from charging towards $+V_{CC}$. Normally the quiscent condition is achieved by connecting pin 2 to $+V_{CC}$ through a resistor. Pin No.6 is connected to ground, through C_{EXT}. (or R) .

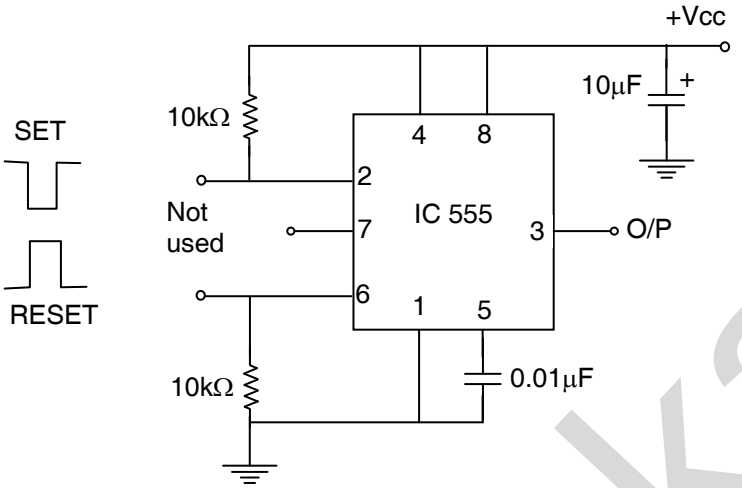
Now to initiate, a negative going trigger pulse is given to pin 2 and its voltage is brought below $v_{CC}/3$. The output of C_2 goes high, thus S = 1 and R = 0. This sets the F/F. $\bar{Q}$ of F/F goes low, internal transistor Q_1 is cut–off and allows C_{EXT} to charge. At the same time $v_0 = +V_{CC}$ due to inverter. Normally pin No.6 is also tied to C_{EXT}. When the C_{EXT}. charges to (2/3) V_{CC}, C_1 comparator output goes high, making S = 0 and R = 1. The F/F is reset and its output $\bar{Q}$ =1. The final output at pin No.3 once again becomes 0 volt. The internal Transistor Q_1 goes into saturation and C_{EXT}. starts discharging through internal Q_1 and some R_{EXT} connected at pin no.7.

Thus basically pin no.2 controls the trigger comparator and voltage at pin No.6 controls the thresh–hold comparator C_1. The output of these 2 comparators are used to control i.e. set or reset the F/F. If F/F is reset then final $v_0 = 0$ and internal Q_1 is in saturation. On the other hand if F/F is set then $v_0 = +V_{CC}$ and internal Q_1 is cut–off.

By connecting different components in different manners at pin nos. 2, 6, and 7, the I.C. can be used as Astable, Monostable, Bistable multivibrator, Schmitt trigger. Similarly varying the voltage at pin no.5 (control voltage), the circuit can be used as a voltage to frequency converter. By giving a negative pulse at pin No.4(Reset) and bringing it down to below +0.4v (Normally this pin is held at $+V_{CC}$), any ongoing operation can be curtailed at any instant.

5. (b) Bistable Multivibrator

As shown in the diagram, pin. No.2 is directly connected to $+V_{CC}$ through 10K R and pin. No.6 is directly connected to ground through 10K R. The outputs of both the comparators are low. R = S = 0 hence F / F is in its last state i.e Reset, $\bar{Q}$ = 1 and hence $V_0 = 0$. This is one of the stable states of bistable multi. & circuit remains in this state unless triggered externally.

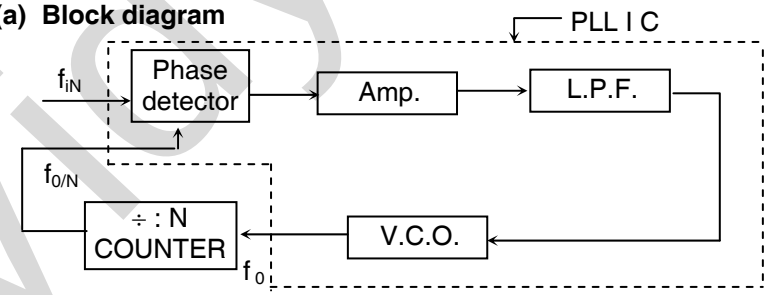


To change the state of v_0 , a negative going pulse is given to trigger pin No.2. The voltage at pin no.2. is brought down below v_{CC}/ 3 and trigger comparator C_2 output goes low. This makes S = 1; R = 0 and the F/F is set, making $\bar{Q}$ = 0. The output v_0 = + V_{CC} ; which is the 2nd stable state of the circuit.

To change this state a positive going pulse is given to thresh–hold pin no.6, So that its voltage is brought above $\frac{+2V_{CC}}{3}$. The output of thresh–hold comparator C_1 goes high, making R = 1, S = 0. This Resets the F/F with $\bar{Q}$ =1. The output once again becomes v_0 = 0. Thus by giving these set and Reset, negative going and positive going pulses respectively in alternate succession the existing state of the circuit can be changed. Since both the states of the circuits are stable in the absence of the triggering pulses, the circuit retains its last value indefinitely and hence it acts as a bistable multivibrator.

5. (c) Frequency Multiplier Synthesizer

(a) Block diagram



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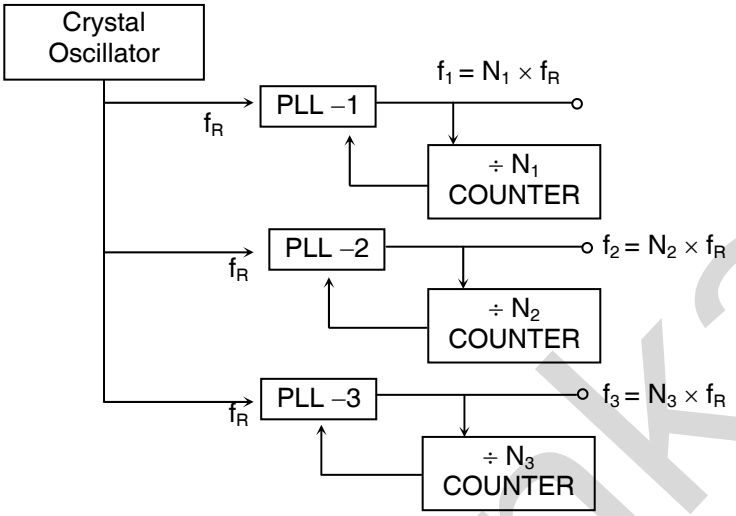
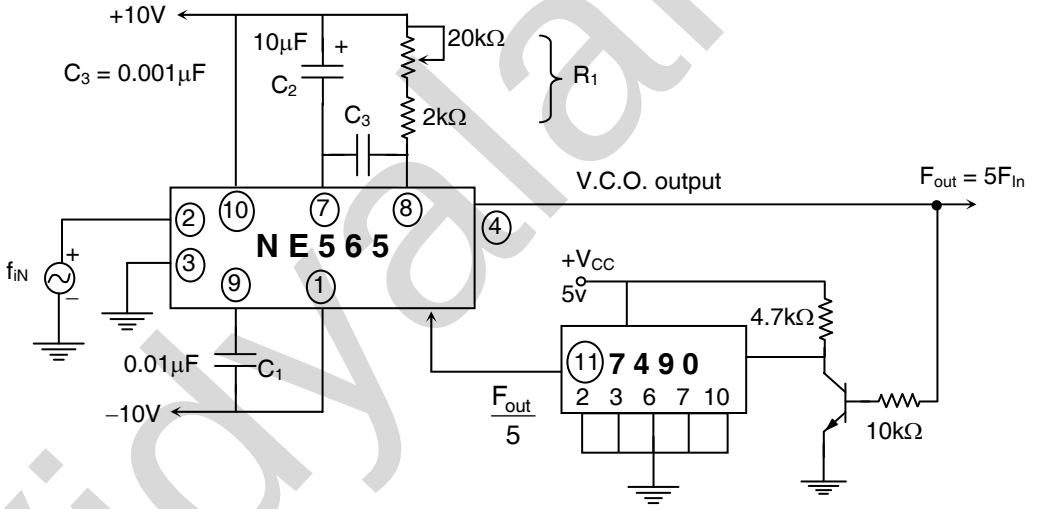
(b) Block diagram for multiple output



(c) Frequency multiplier circuit diagram



Normally V. C. O. output signal available at pin no. 4 is directly shorted to pin no.5, thus connecting it to internal phase detector. But in this case a divide by N (÷N) counter is introduced between pin nos. 4 & 5. Due to this if f_0 is the centre frequency of V.C.O. then the frequency of the signal fed to phase detector in f_0/N.

At pin No. 2 a very accurate frequency of f_R from crystal oscillator is fed. The job of PLL is to compare these 2 input frequencies and lock them. If F_R falls within the lock–range of PLL, the 2 frequencies lock to each other and become equal.

In this case $\frac{f_0}{N} = f_R$

i.e. $f_0 = N \times f_R$. Thus by selecting the modulus of the counter (N), the reference crystal oscillator frequency can be multiplied by any integer. As shown in the

circuit, along with PLL I.C. 565, a decade counter I.C. 7490 is used to do this frequency multiplication.

As shown in the 2nd diagram, by using no. of PLL I.C's and different modulo (N_1, N_2, N_3) counters, at a time no. of different frequency standards can be obtained which are integral multiples of original crystal oscillator frequency f_R.
In this circuit, $f_1 = N_1 \times f_R$; $f_2 = N_2 \times f_R$; $f_3 = N_3 \times f_R$.

5. (d) Operation of phase detector and role of VCO in PLL

1) **V.C.O.** : It consists of voltage controlled current source which supplies equal magnitude of charging and discharging currents to an externally connected (pin no.9) timing capacitor C_{EXT}. A timing R_{EXT}. is connected between pin no.8 and $+V_{CC}$. The rest of circuit consists of Schmitt trigger with a differential amplifier output circuit. The basic function of V. C. O. is to produce square wave oscillations whose frequency depends upon (i) R_{EXT}. (ii) C_{EXT}. (iii) Control voltage V_f.

2) **Phase detector :** It consists of differential amplifier pairs provided with current sink bias source. The output voltage of phase detector is limited by diodes to a max of $\pm$ 0.7 volts, so as to limit the effect of noise signal. The phase detector has s balanced output and is supplied to Differential (D. C.) amplifier.

   The basic job of phase detector is to compare the input signal f_{IN} with free running f_0 of V.C.O. Initially it generates a very frequency output signal having a D.C. average value. This acts as a control signal to V. C. O. so that f_0 becomes equal to f_{IN}. Once the frequency lock is obtained, phase detector now generates D. C. voltage proportional to cos ϕ where ϕ is the phase difference between 2 locked signals. This signal changes the phase of V.C.O. signal till it is in quadrature (90°) with respect to v_{in}.

5. (e) Centre frequency(free running frequency)

Centre frequency is defined as the frequency at which internal V. C. O. oscillates when no input signal is given to PLL. It is given by $f_0 = \dfrac{1.2}{4R_{EXT.}\,C_{EXT}}$ where R_{EXT}. & C_{EXT} are connected at pin no.8 and 9 of PLL I.C. NE/SE 565. This f_0 is normally adjusted at the centre of the input frequency range.

Pull in time : The time measured from the instant the input signal is given to the instant at which the 2 frequencies f_{IN} and f_0 are locked for the first time, is defined as the pull in time of PLL.

Transfer characteristics

From the transfer characteristics shown in figure 2,

(i) It is clear that for PLL to work satisfactorily, f_{iN} and f_0 should be sufficiently close to each other.

(ii) At the start of the operation, to acquire a lock for the first time, f_{IN} must come still closer to f_0. Thus f_{IN} must be equal to f_1 (if f_{IN} is increasing) or equal to f_2 (if f_{IN} is decreasing), then only a lock will be acquired for the first time. Thus $(f_2 - f_1) = 2\Delta f_{CR}$ is known as Capture range.

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(iii) Once the lock has acquired for the first time (i.e. $f_{IN} = f_0$) then the lock is maintained even if the f_{IN} now goes beyond the capture range. For this f_{IN} must lie between f_3 and f_4. where $(f_4 - f_3) = 2\Delta f_{CL}$ is the lock range of PLL.

(iv) The lock range is always greater than the capture range. The PLL can lock to an input signal over typically ± 60% B. W. with respect to f_0 as the centre frequency. The lock range generally increases with an increase in the magnitude of the input signal but decreases with an increase in supply voltage. Normally the operating 'f' range of PLL is restricted to lock range. To avoid the effect of noise signal, a negative feedback is used by connecting a resistor between pin nos. 6 and 7.

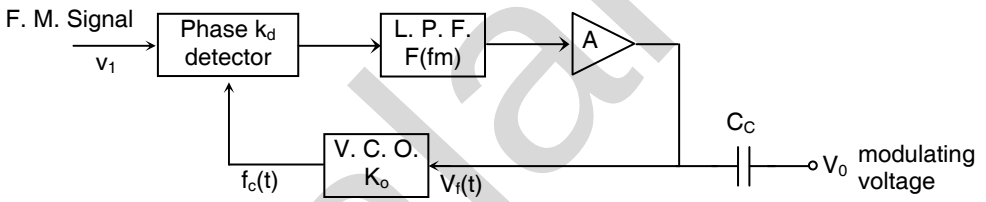
(v) Capture range is typically % of lock range. For acquiring the lock, first time, f_{IN} must come within the capture range of PLL. Thus capture range refers to how close input signal frequency must come to the free running f_0 of V. C. O. before the first lock can occur.

5. (f) FM demodulator using PLL

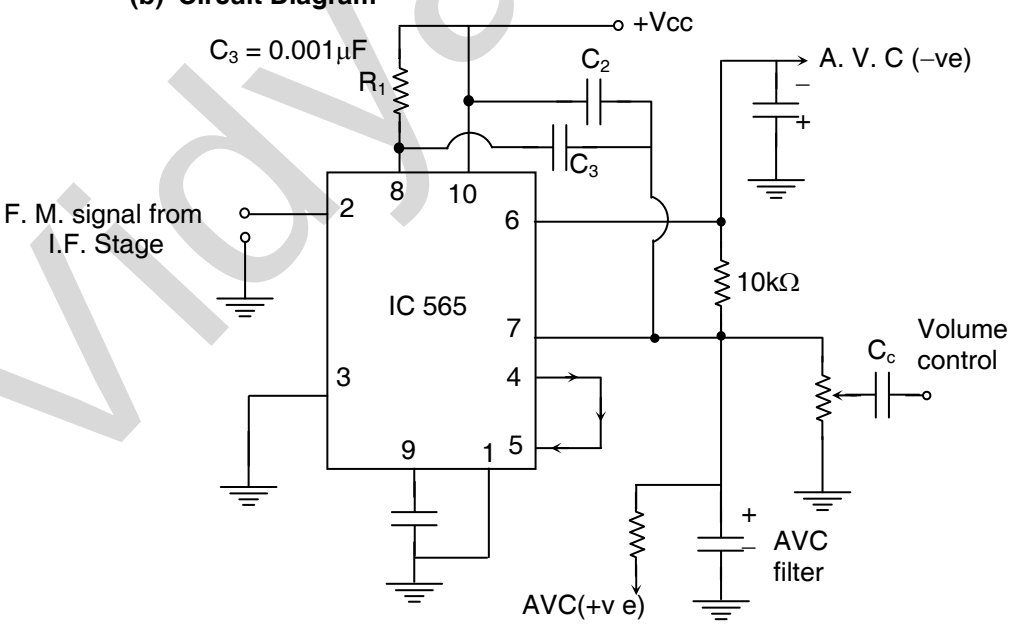
PLL Applications

- **F.M. demodulator / F.M. detector**

(a) Block diagram



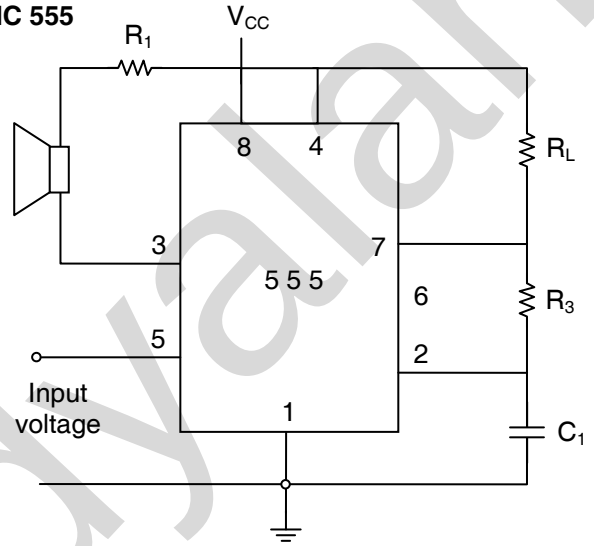
(b) Circuit Diagram



F.M. signal from the I. F. amplifier is a single ended signal. This signal is applied to pin no.2 and pin no.3 is grounded. R_{EXT}. and C_{EXT}. at pin no.8 and 9 are so selected that the free running frequency becomes almost equal to the I. F. frequency of F.M. receiver (i.e. 10.7MHz). Now C_2 connected between pin no.7 and $+V_{CC}$ along with internal resistor 3.6kΩ forms the L. P. F. of PLL. The value of C_2 is so chosen that the B.W. of F. M. I. F. signal falls in the pass band of L. P.F. At the start, V.C.O. f_0 is locked to F.M.I.F. frequency of 10.7MHz. Now as the input signal is frequency modulated, its frequency varies about I. F. frequency. Since this variation falls in the lock range of PLL, the V. C. O. frequency follows the input frequency and remains locked with it. The output of the phase detector also follows this change in frequency and hence this output is the audio signal which has frequency modulated the carrier signal.

Thus at pin. No.7, de–modulated audio signal is available which is dropped across external volume–control. This audio signal is then applied to audio power amplifier through a coupling capacitor. At the same time 2 A. V. C. external filters are used to generate positive and negative D. C. voltage which is used for A. V. C. control.

6. (a) V_{co} using IC 555



- 555 is used as astable multivibrator.
- The difference of this circuit with the basic 555 astable circuit is that its 555's pin 5 is used to an external voltage source.
- Pin 5 is the 555's control voltage pin, which allows the user to directly adjust the threshold voltage to which the pin2/pin6 input voltage or compared by the 555's internal compartment.
- Since the output of these comparators control the internal the flip-flop that toggles the output of the 555 adjusting the pin 5 control voltage also adjusts the frequency at which the 555 toggles output.
- Increasing the input voltage at pin 5 decreases the output oscillation frequency while decreasing this input voltage increase the output oscillator frequency.

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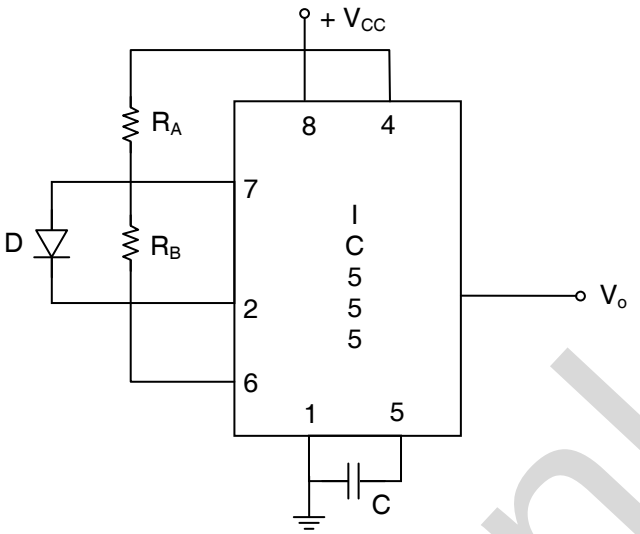
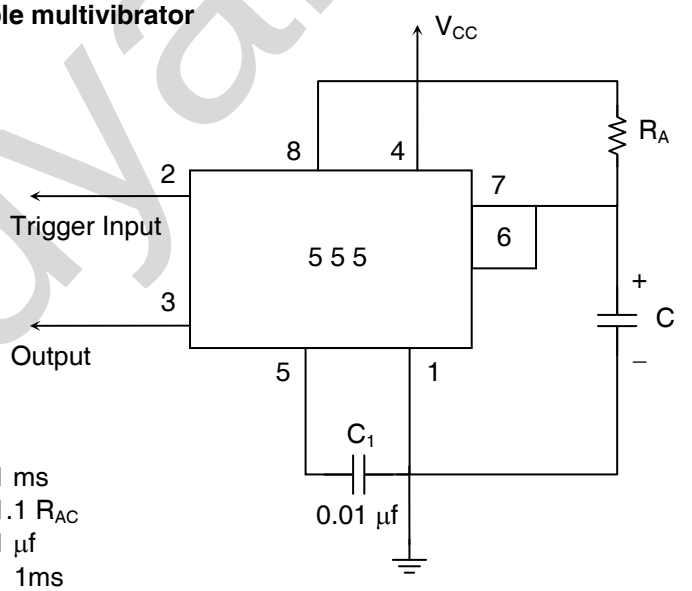
6. (b) Square wave generator using IC 555



- External diode is connected between pin 2 and due to this now the on time is changed to
  $T = 0.693 (RA) C$
  because now during discharging the R_B is shorted by diode D.
- So frequency $f = \frac{1}{0.693(RA).C}$

6. (c) For monostable multivibrator



$T_P = 1$ ms

$\therefore$ $1\text{ms} = 1.1\ R_{AC}$

Let $C = 1\ \mu f$

$$R_A = \frac{1\text{ms}}{1.1 \times 1\mu f}$$

$R_A = 909.01\ \Omega$

Take $R_A = 1\ k\Omega$

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6. (d) RC Phase Shaft oscillator for frequency 200 Hz

i) $\because \quad f_0 = \dfrac{1}{2\pi\sqrt{6}\,RC} = \dfrac{0.065}{RC}$

Let $C = 0.1\ \mu F$

$$R = \frac{0.065}{(200)(10^{-7})}$$

$= 3.25\ k\Omega$

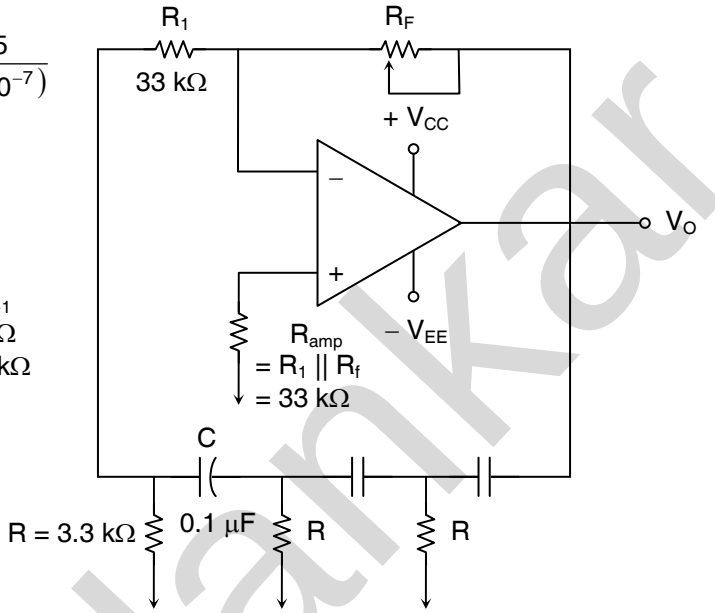
Use $R = 3.3\ k\Omega$

ii) $\because \quad \left|\dfrac{R_F}{R_1}\right| = 29$

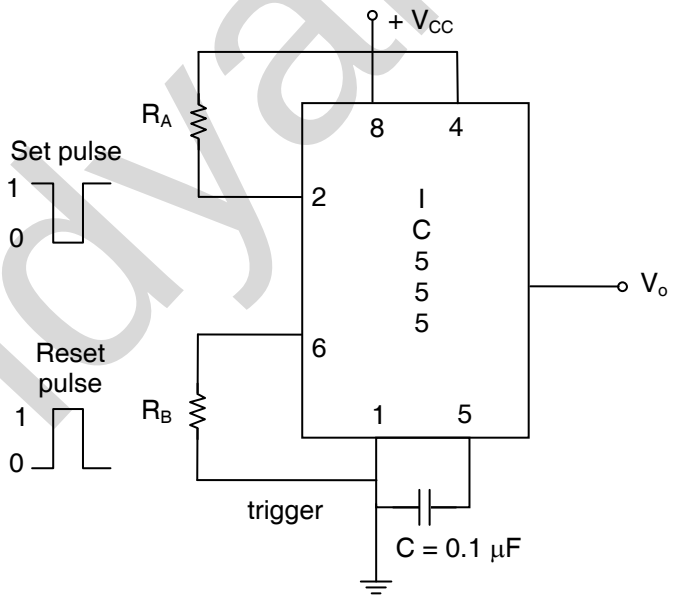
$R_F = 29\ R_1$

Let $R_1 = 33\ k\Omega$

$R_F = 957\ k\Omega$



6. (e) Bistable multivibrator using IC 555



- Bistable multivibrator has two stable state.
- Once it is reached in one stable state it is continue to be in that stable state until external excitation.

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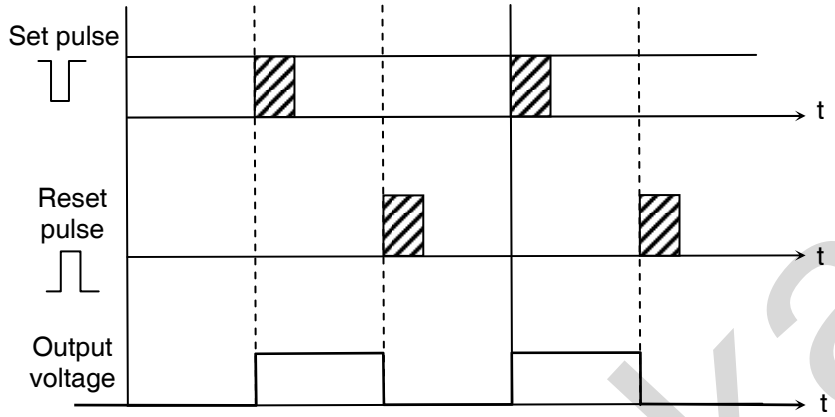
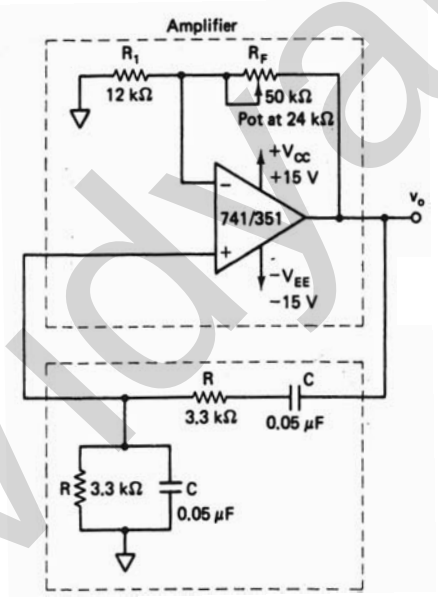
Waveforms



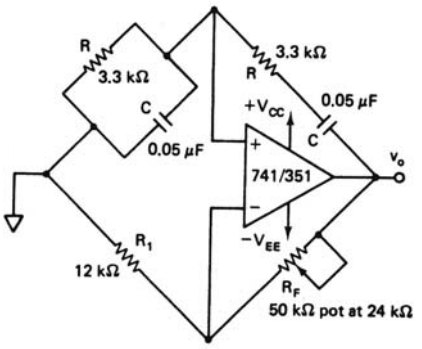
- When negative going pulse is applied at the input the upper comparator output is high and lower comparator output is low which will set flip flop so a = 1, $\bar{a}$ = 0. In this situation we get high output voltage.
- When reset pulse (Positive going pulse) applied the output of upper comparator is low and low comparator is high which will reset flip-flop a = 0, $\bar{a}$ = 1 we get saturated output voltage.

6. (f) Wein bridge Oscillator

Circuit Diagram :



Equivalent Circuit :



Operation :

Because of its simplicity and stability, one of the most commonly used audio–frequency oscillators is the Wein Bridge. The figure shows the Wein bridge oscillator in which the Wein bridge circuit is connected between the

amplifier input terminals and the output terminal. The bridge has a series RC network in one arm and a parallel RC network in the adjoining arm. In the remaining two arms of the bridge, resistors R_1 and R_F are connected. The phase angle criterion for oscillation is that the total phase shift around the circuit must be 0. This condition occurs only when the bridge is balanced, that is, at resonance. The frequency of oscillation f_o is exactly the resonant frequency of the balanced Wien bridge and is given by

$$f_0 = \frac{1}{2\pi RC} = \frac{0.159}{RC}$$

assuming that the resistors are equal in value, and the capacitors are equal in value in the reactive leg of the Wien bridge. At this frequency the gain required for sustained oscillation is given by

$$A_v = \frac{1}{\beta} = 3$$

That is, $1 + \frac{R_F}{R_1} = 3$

or $\frac{1}{SC}$

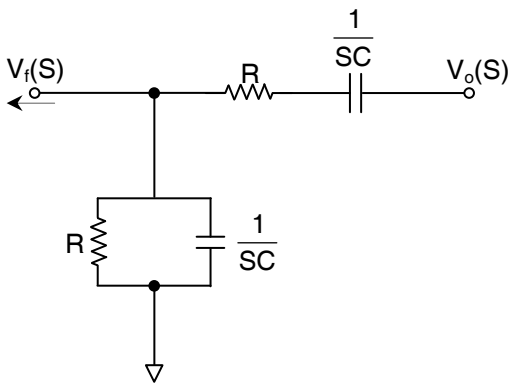
Derivation :

First consider the feedback circuit of the Wien bridge oscillator of the figure above. The circuit is transformed in the S domain and redrawn in the figure below. Using the voltage–divider rule,

$$V_f(S) = \frac{Z_p(S)\,V_o(S)}{Z_p(S) + Z_s(S)}$$

where $Z_p(S) = R \| \frac{1}{SC} = \frac{R}{RSC+1}$

$$Z_s(S) = R + \frac{1}{SC} = \frac{RCS+1}{SC}$$



Therefore, substituting $Z_p(S)$ and $Z_s(S)$ values, we get

$$V_f(S) = \frac{(RCS)\,V_o(S)}{(RCS+1)^2\,RCS}$$

or $B = \frac{V_f(S)}{V_0(S)}$

$$= \frac{RCS}{R^2C^2S^2 + 3RCS + 1} \quad \ldots (1)$$

Next consider the op–amp part of the Wien bridge oscillator. The circuit is redrawn in the figure below.

The voltage gain A_v of the op–amp is

$$A_v = \frac{V_o(S)}{V_f(S)} = 1 + \frac{R_F}{R_1} \quad \ldots (2)$$

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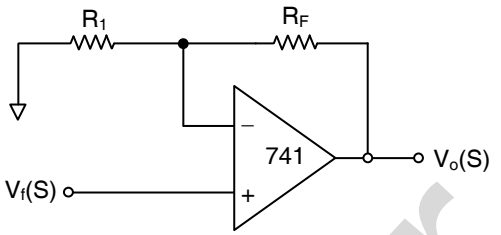
Finally, the requirement for oscillation is

$$(A_v)\,(B) = 1$$

Therefore, using Equation 1 and 2, we have

$$\left(1+\frac{R_F}{R_1}\right)\frac{RCS}{R^2C^2S^2+3RCS+1} = 1$$



Op–amp part of the Wien bridge oscillator

Substituting S = jω in this equation and then equating the real and imaginary parts, we get the frequency of oscillation f_o and the gain required for oscillation, as follows:

$$\left(1+\frac{R_F}{R_1}\right)jRC\omega = \left(-R^2C^2\omega^2\right)+j\left(3RC\omega\right)+1$$

$$\omega^2 = \frac{1}{R^2C^2} \quad (\text{real part})$$

or $$f_0 = \frac{1}{2\pi RC}$$

and $$\left(1+\frac{R_F}{R_1}\right)jRC\omega = j\left(3RC\omega\right) \qquad \text{(imaginary part)}$$

or $$1+\frac{R_F}{R_1} = 3$$

$$R_F = 2R_1$$

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