T.Y. Diploma : Sem. VI
[EJ/ET/EX/EN/EI/IE]
Very Large Scale Integration

Time : 3 Hrs. Prelim Question Paper **Marks : 100**

Instructions :(1) All questions are compulsory.
(2) Answer each next main question on a new page.
(3) Illustrate your answers with neat sketches wherever necessary.
(4) Figures to the right indicate full marks.
(5) Assume suitable data, if necessary.
(6) Mobile Phone, Pager and any other Electronic Communication devices are not permissible in Examination Hall.

1. (a) Attempt any **THREE** questions. **[12]**
(i) Differentiate between Xiliv and Atmel series architecture of CPLD. (four points)
(ii) Draw NAND and NOR gates using NMOS.
(iii) Write any two pro's and any two con's of VHDL.
(iv) Give the difference between Moore and Mealy machines (four points).

1. (b) Attempt any **ONE** questions. **[6]**
(i) Explain CZ process for wafer fabrication, with neat diagram.
(ii) Write the VHDL program to implement 4 bit adder.

2. Attempt any **FOUR** questions. **[16]**
(a) Define the following terms :
(i) Meta stability (ii) Set-up time (iii) Hold time (iv) Fan-out
(b) Compare FPGA and CPLD.
(c) Explain oxidation and diffusion process in fabrication process.
(d) What are the advantage of twin-tub process of CMOS fabrication?
(e) List the types of FSM. Draw labelled diagram of each.
(f) Draw the HDL design flow for synthesis. Write the steps in the flow.

3. Attempt any **FOUR** questions. **[16]**
(a) Design clocked sequential circuit using Toggle flip-flop to count from 00 to 11 (2 bit counter).
(b) Compare BJT and CMOS (any four).
(c) Write the VHDL code for 3:8 decoder.
(d) Draw NAND gate using CMOS transistors.
(e) Explain the estimation of resistance of channel for MOSFET (Sheet Resistance).
(f) Draw the ASIC design flow and explain it.

4. (a) Attempt any **THREE** questions. **[12]**
(i) Explain with syntax.
(1) Entity (2) Architecture
(ii) Explain the following terms :
(a) Event scheduling (b) Simulation cycle
(iii) List the any four logical operators in VHDL.
(iv) List the advantages and disadvantages of VHDL.

(b) Attempt any **ONE** questions. **[6]**
(i) Draw the complete block diagram of CPLD and explain the same.
(ii) List and explain the main steps carried in typical n-well, CMOS fabrication process with neat sketches.

5. Attempt any **FOUR** questions. **[16]**

(a) Differentiate between asynchronous and synchronous logical circuit.
(b) Explain with the syntax : (i) Signal (ii) Variable.
(c) Draw the general FPGA chip architecture and explain the same.
(d) Draw the CMOS inverter characteristic and explain it.
(e) Draw the functional block architecture of Xilinx CPLD.
(f) What is event scheduling and zero modelling.

6. Attempt any **FOUR** questions. **[16]**

(a) Write VHDL code for FULL ADDER.
(b) Define sensitivity list. State any two VHDL syntax in which sensitivity list is defined.
(c) Draw the simulation cycle and label it.
(d) Draw HDL design flow for synthesis.
(e) Execute the following equation by the circuit with CMOS logic.
D = [(A·B) + (C·D)]

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Paper Discussion Schedule for: T.Y. Diploma Sem. VI

Date	Day	Timing	Centre
14 April 2018	Saturday	8 a.m. to 10 a.m.	Dadar
14 April 2018	Saturday	11 a.m.to 1 p.m.	Thane