S.Y. Diploma : Sem. III
[CO/CM/IF/CD/CW]

Digital Techniques

Time: 3 Hrs.] Prelim Question Paper **[Marks : 100**

Instructions : (1) **All** questions are **compulsory**.
(2) Illustrate your answers with **neat** sketches wherever necessary.
(3) Figures to the **right** indicate **full** marks.
(4) Assume suitable data, if **necessary**.
(5) Mobile Phone, Pager and any other Electronic Communication devices are **not** permissible in Examination Hall.

1. (a) Attempt any **SIX** of the following : **[12]**

(i) Derive AND gate and OR gate using NAND gates only.
(ii) Define Duality theorem and give example.
(iii) List any four Boolean laws.
(iv) Define any two specifications of ADC.
(v) Draw the symbol and truth lable of AND and OR gate.
(vi) Define with respect to digital ICs
(1) Propagation delay (2) Noise immunity
(vii) Which are the universal gates? Why they called it?
(viii) Define any two specifications of DAC.

(b) Attempt any **TWO** of the following : **[8]**

(i) Draw symbol and write truth table of 2 : 1 MUX. Also draw the block diagram of 8 : 1 mux.
(ii) Convert the following:
(1) $(11001)_2 = (\ ?\ )_{10}$
(2) $(10101)_2 = (\ ?\ )_8$
(3) $(37)_8 = (\ ?\ )_2$
(4) $(5AC) = (\ ?\ )_2$
(iii) Draw truth table of 3 inputs EX-OR gate. Draw its symbol. Also give its output expression.

2. Attempt any **FOUR** of the following : **[16]**

(a) Draw logical symbol, truth table and logical expression for NAND and NOR gate.
(b) Perform the following binary operations.
(i) 111.01 × 110
(ii) 11001 ÷ 101

(c) For the given K-map in Figure, write minimized SOP expression and for the same draw NAND-NAND logic circuit.

	$\bar{C}\bar{D}$	$\bar{C}D$	CD	$C\bar{D}$
$\bar{A}\bar{B}$	0	1	0	0
$\bar{A}B$	1	1	1	0
AB	1	1	1	0
$A\bar{B}$	0	0	1	0

(d) Simplify the following equation using k–map and realize it using logic gates.
$Y = \Sigma m(0, 1, 2, 3, 8, 10) + \Sigma d(5, 7)$.

(e) Draw 16:1 MUX using 4:1 MUX

(f) Perform the following substraction using 2's complement method.
(i) $(01000)_2 - (01001)_2$ (ii) $(01100)_2 - (00011)_2$

(g) Design a full adder using half adder.

3. Attempt any **FOUR** of the following : **[16]**

(a) Convert the expression $Y = AB + A\bar{C} + BC$ into the standard SOP form.

(b) Draw logic diagram of 1:4 demultiplexers. Write truth table of it.

(c) Reduce the given logic expression using Boolean laws and draw NAND logic circuit.
$Y = A + \bar{A} \cdot B + A \cdot B$

(d) For the given K-Map in figure, write the POS expression and draw NOR-NOR logic circuit for same.

	$\bar{C}\bar{D}$	$\bar{C}D$	CD	$C\bar{D}$	
$\bar{A}\bar{B}$	0	1	1	1	
$\bar{A}B$	0	0	0	1	
AB	1	1	0	0	
$A\bar{B}$	1	1	0	0	

(e) Minimize the following equation using k–map.
(i) $Y = \Sigma m(0, 1, 2, 4, 5, 6)$ (ii) $Y = \prod m(0, 2, 4, 5)$.

(f) Explain working of PIPO with neat logic diagram and timing diagram.

(g) Obtain an 1 : 8 demultiplexer using 1 : 4 demultiplexer.

(h) Explain the functions of 'preset' and 'clear' inputs in flip-flops.

4. Attempt any **FOUR** of the following : **[16]**

(a) Classify the memories and explain ROM.

(b) State any four specifications of A to D converter.

(c) Construct D-flip flop using R-S flip flop and explain it's working along with truth table.

(d) Describe working of RS ff using NAND gates only.
(e) Draw and explain D flip-flop using SR flip-flop. Also draw truth table.
(f) Draw neat circuit diagram of clocked JK flip-flop using NAND gates. Give its truth table and explain race around condition.

5. Attempt any **FOUR** of the following : **[16]**

(a) Draw the logic diagram of D type flip flop using NAND gates. Write its truth table.
(b) Draw Master- slave J-K flip-flop and explain it's working.
(c) Define 'Modulus of counter'. Determine number of flip flops to be used in MOD-21 counter.
(d) Compare combinational logic circuit and sequential logic circuit (any 4 pts)
(e) Describe block diagram of digital comparator and write truth table of 2 bit comparator.
(f) List different types of flip-flop. Draw the diagram of master Slave JK flip-flop.
(g) Draw the diagram of serial in parallel out (SIPO) shift register. Also draw timing diagram.
(h) State different applications of flip flops.
(i) Draw and explain SISO with truth table and timing diagram.

6. Attempt any **TWO** of the following : **[16]**

(a) (i) Draw the circuit diagram of successive approximation type A to D converter and describe its working.
(ii) A D to A converter has a full scale analog output of 12V with 4 bit binary inputs. Find the voltage corresponding to each analog step.
(b) (i) List four applications of flip flops.
(ii) Compare synchronous and asynchronous counter on any two points.
(iii) Convert JK- flip flop in to T-flip flop. Write it's truth table and explain
(c) (i) Convert the following SOP equation into standard SOP equation.
$Y = AB + \overline{A}B + A\overline{B}\,\overline{C}$
(ii) List any four applications of multiplexer and implement the following logic expression using 16:1 MUX.
$Y = \Sigma m(0, 3, 5, 6, 7, 10, 13)$.
(d) Draw block diagram and truth table of 1:4 demultiplexer.
(e) (i) With suitable diagram describe successive approximation ADC.
(ii) List any four specifications of ADC.

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