**Q.1(a) Attempt any SIX of the following : [12]**

**Q.1(a) (i) What are transistor biasing circuits and name the different biasing circuits? [2]**

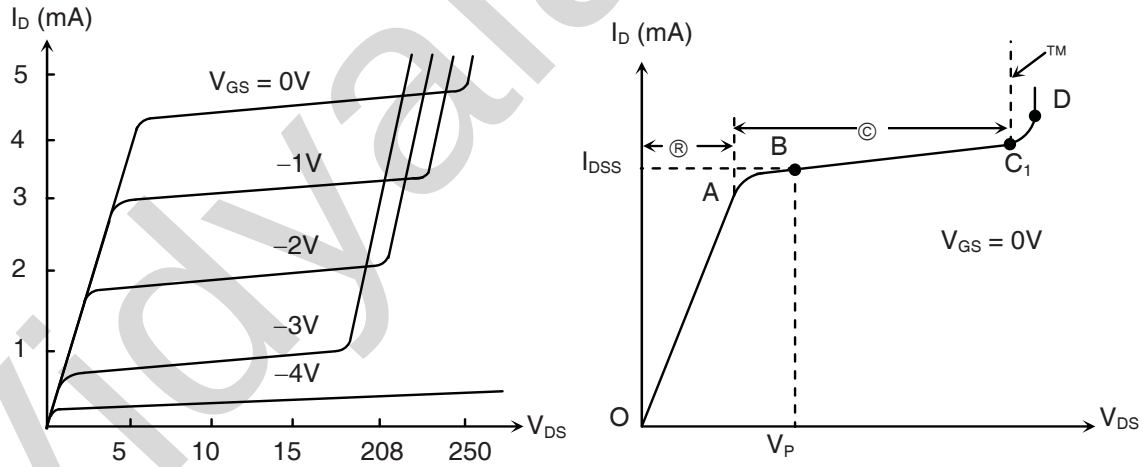
**(A)** A circuit used for establishing Quiscent operating point (Q) in the centre of active region to avoid distortion is defined as transistor biasing circuit. For this purpose, normally circuit uses one external d.c. supply, few resistors and may be 1 capacitor. By choosing their values properly, B – E junction is forward biased and B – C junction is reverse biased.

Some of the transistor biasing circuits used are

1) Fixed Biased circuit
2) Base biased with collector feedback
3) Base biased with emitter feedback
4) Voltage (or potential) divider
5) Emitter biased

**Q.1(a) (ii) Draw Drain (Output) characteristics of N–channel JFET & show different regions of operation on it. [2]**

**(A)**




The regions of operation are shown in characteristics drawn for $V_{GS}$ = OV.

1) *Ohmic region OA* : $I_D$ v/s $V_{DS}$ and obeys ohm's law.
2) *Pinch–off or saturation region BC* : $I_D$ remain constant at maximum value even though $V_{DS}$ is increased. Current $I_D$ in this region is given by schockly's equation

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

3) *Breakdown region CD* : $I_D$ starts increasing very rapidly due to breakdown of gate to source junction due to avalanche effect. This region of operation should be avoided to reduce damage to JFET.

**Q.1(a) (iii) Define multi-stage amplifier and state its necessity. [2]**

**(A) Multi-Stage Amplifier**

A circuit in which number of single stage amplifiers are connected in cascade (in series) such that output of the previous amplifier is connected to the input of the next amplifier is defined as multi-stage amplifier.

A single stage voltage amplifier is not capable of giving too large voltage gain. Sometimes input signals are very weak, in such cases they are required to be amplified more. For this purpose multi-stage amplifiers are used.

**Q.1(a) (iv) Define intrinsic standoff ratio (η) of UJT. [2]**

**(A) Intrinsic stand-off ratio (η)** is one of the important characteristics of UJT and given by

$$\eta = \left.\frac{r_{B_1}}{r_{BB}}\right|_{I_E=0} = \left.\frac{r_{B_1}}{r_{B_1}+r_{B_2}}\right|_{I_E=0}$$

It is defined as the ratio of internal resistance between $B_1$ and E to the total internal resistance between 2 base terminals provided emitter current $I_E = 0$. The value of is given by $0.5 < \eta < 0.8$ and typically $\eta = 0.65$ or o.7.

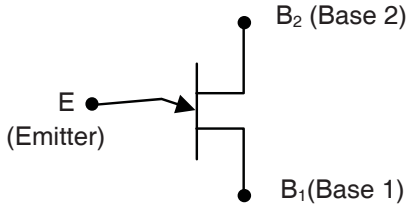
**Q.1(a) (v) Give the symbol of UJT and state why it is called uni-junction transistor. [2]**

**(A) UJT**

i) From the construction it is clear that the device has one (uni) P – N junction.

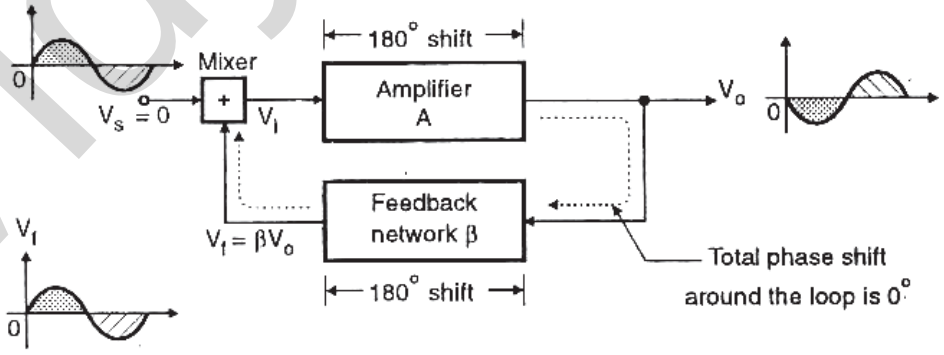
ii) Like transistor it is 3 terminal device. The terminals are known as Base 1, Base 2, Emitter.

Due to the above 2 reasons it to called uni-junction transistor.




**Q.1(a) (vi) State Barkhausen criterion on oscillation. [2]**

**(A) Barkhausen Criterion**




- For an oscillator the input voltage $V_s$ is absent i.e. $V_s = 0$ and the feedback signal $V_f$ is supposed to maintain the oscillations. Therefore substitute $V_s = 0$ into Equation (5) to get,

$$V_i(1 - A\beta) = 0$$

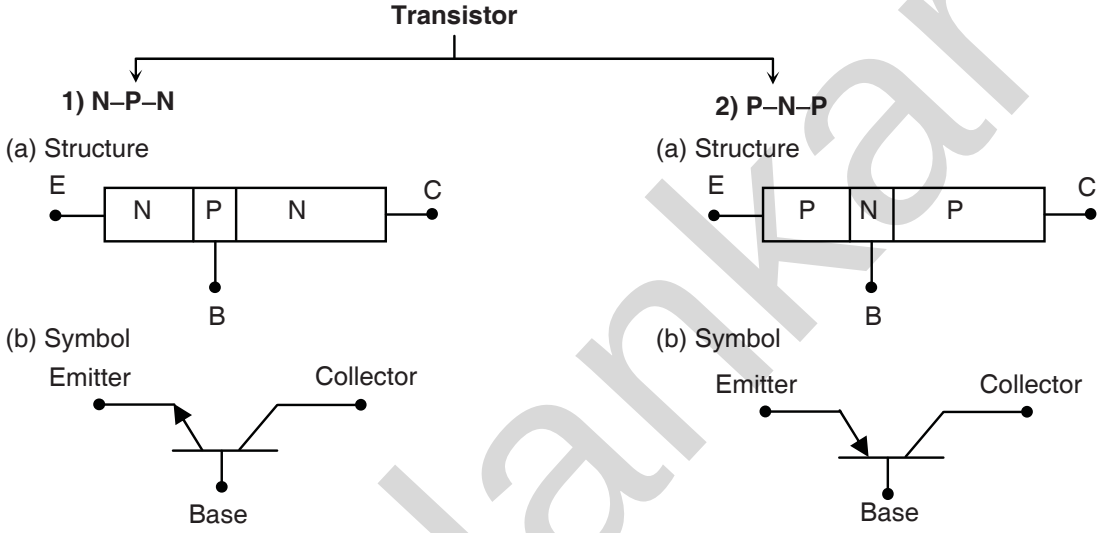
or $$A\beta = 1$$

This condition must be satisfied in order to obtain sustained oscilations.

- With an inverting amplifier introducing a 180° phase shift between $V_i$ and $V_o$, the feedback network must introduce another 180° phase shift to ensure that $V_i$ and $V_f$ are in phase.
- These two conditions which are required to be satisfied to operate the circuit as an oscillator are called as the "Barkhausen criterion" for sustained oscillations.

**Q.1(a) (vii) State the two types of transistor and give their symbols. [2]**

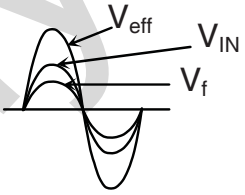
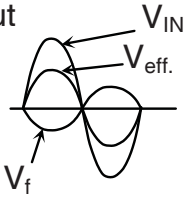
**(A)** Depending upon the type of 3 semiconductor regions used, transistor is classified into following 2 types. Their symbols are also given.




**Q.1(b) Attempt any TWO of the following : [8]**

**Q.1(b) (i) Give the comparison between –ve feedback and +ve feedback. [4]**

**(A) Comparison between –ve feedback and +ve feedback**

| | +ve feedback | –ve feedback |
|---|---|---|
| 1) | $V_{IN}$ and $V_f$ are in phase hence effective input voltage increases   | $V_{IN}$ and $V_f$ are 180° out of phase hence effective input voltage decreases.   |
| 2) | Voltage gain increases $A_{fb} = \frac{A_v}{1 - A_v\beta}$ | Voltage gain decreases $A_{fb} = \frac{A_v}{1 + A_v\beta}$ |
| 3) | Distortion increases. | Distortion decreases. |
| 4) | Noise in the output signal increases. | Noise in the output signal decreases. |
| 5) | Circuit becomes unstable, starts oscillating and produces new output signal of different frequency. | Stability of amplifier improves since $A_{fb}$ remains constant because it becomes independent of transistor parameter. |
| 6) | It is used in all oscillators. | It is used in amplifiers. |

**Q.1(b) (ii) Explain self-bias circuit used in JFET.** **[4]**

**(A)** Voltage at the gate terminal $V_G = -I_G R_G$ but $I_G = 0$

$\because$ $R_{IN}$ of JFET very high.

$\therefore$ $V_G = 0$

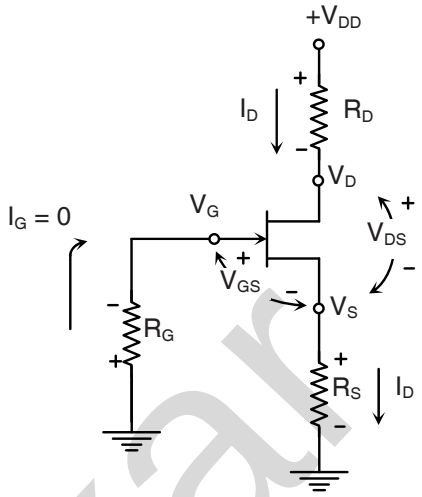
Now $V_s = V_G - V_{GS} = -V_{GS}$

By Ohm's law $I_D = \dfrac{V_S}{R_S} = \dfrac{-V_{GS}}{R_s}$

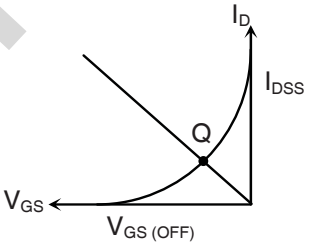
$\therefore$ $V_{GS} = -I_D R_s$

Thus voltage drop across $R_s$ reverse biases gate to source P–N junction.

$\because$ $I_{DQ} = \dfrac{-V_{GS}}{R_S}$ … (i)




A graph can be plotted (straight line) between $I_D$ and $-V_{GS}$. On the same graph, transfer characteristics is plotted and as shown Q point can be selected in the centre by selecting proper value for $R_s$.




Similarly applying K.V.L. to the output we get

$$\sum \text{All voltages} = 0$$

$\therefore$ $+ V_{DD} - I_D R_D - V_{DS} - I_D R_s = 0$

$\therefore$ $V_{DD} - I_{DQ}(R_D + R_S) = V_{DSQ}$ … (ii)

Equations (i) & (ii) establish Q point.

This is one of the best biasing network for JFET and is used because of the following reasons.

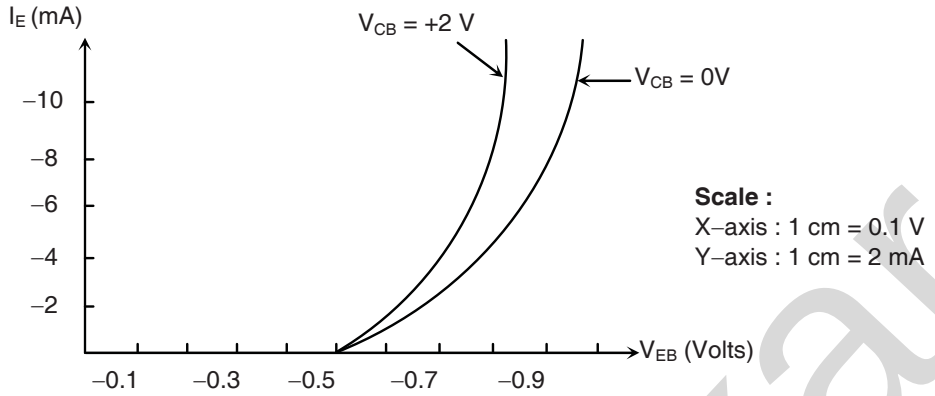
(1) Uses only one d.c. supply + $V_{DD}$

(2) Requires few component

(3) Q point is stable because of following two reasons.
   (i) Q point independent of FET parameter.
   (ii) Due to negative feedback introduced by voltage drop $I_D R_S$. Assume that due to temperature variation, $I_D$ increases. This increase voltage drop $I_D R_s$. Now $V_{GS} = -I_D R_s$ & hence reverse bias on gate–source junction increases. This reduces $I_D$ and is brought back to original value. Exactly reverse action takes place if $I_D$ decreases. Hence due to this negative feedback $I_D$ and Q point remains stable.

**Q.1(b) (iii) Draw input characteristics for N–P–N transistor in common–Base configuration & explains it. [4]**

**(A)** Input characteristics : $I_E$ v/s $V_{EE}|_{V_{CB}=\text{ constant}}$

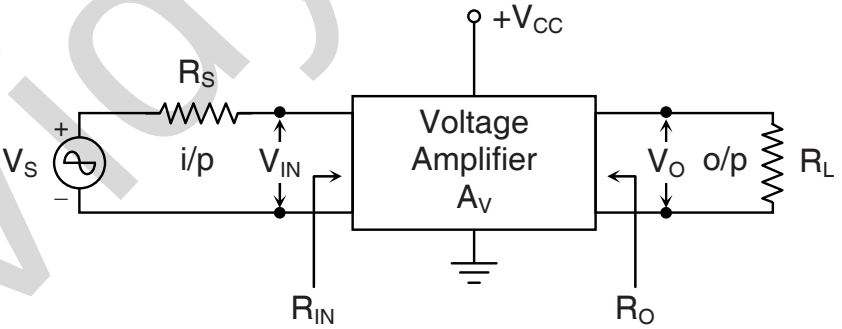



1) Transistor is working in active region hence its input P–N (B–E) junction is forward biased. Hence the input characteristics is exactly identical to forward characteristics of P–N junction.
2) By convention, $V_{EB}$ and $I_E$ are negative but the curve is plotted in 1st quadrant.
3) characteristics are plotted by keeping output voltage $V_{CB}$ constant. Hence 2 curves are plotted by keeping $V_{CB}$ = 0 & then $V_{CB}$ = 2V as constant.
4) As $V_{CB}$ increases in positive direction then the curve shifts slightly towards left since less input voltage is now required for sending same input current.

**Q.2 Attempt any FOUR of the following : [16]**

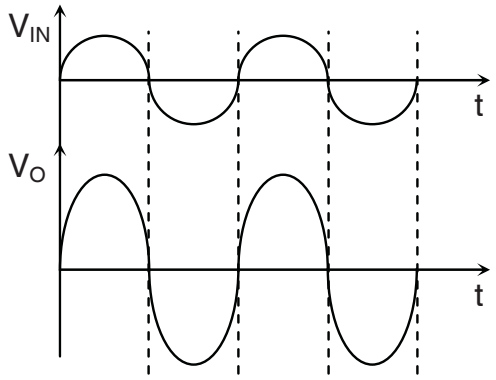
**Q.2(a) Draw block diagram of voltage amplifier. Show important parameters of amplifier on it and state the requirements of good voltage amplifier. [4]**

**(A) Voltage Amplifier**




$A_V$ = voltage gain of the amplifier
$R_{IN}$ = input resistance of the amplifier
$R_O$ = output resistance of the amplifier
$V_S$ = A.C. signal from function (or signal) generator $V_O > V_{IN}$ without distortion

**Wave form :**




**Requirements of good voltage amplifier :**

i) *Voltage gain* ($A_V\uparrow$) : It should be as high as possible or It must be sufficient which depends upon the application.

ii) *Input resistance* ($R_{IN}\uparrow$) : It is measured in ohms. Ideally it must be infinite, practically it must be as high as possible. This avoids the loading (decreasing) of input signal.

iii) *Output resistance* ($R_O\downarrow$) : It is measured in ohms. Ideally it must be zero, practically it must be as low as possible. This avoids the loading (decreasing) of the voltage signal present at the output terminals.

iv) *Frequency response* (or Band – width) : It is measured in $H_z$ or $KH_z$ or $MH_z$. Ideally it must be infinite, practically it must be sufficient for the required application. Basically Band – width represents the range (group) of frequencies which are amplified properly by the amplifier.

v) *Distortion* : It must be as low as possible. If the shape of the amplified output voltage $V_0$ is different from the shape of input voltage then we say distortion is present. This must be avoided in any amplifier.

vi) *Stability* : This must be good so that Q point remains stable in the centre of active region under D.C. conditions.

**Q.2(b) Give the comparison between 3 configurations of transistor. [4]**

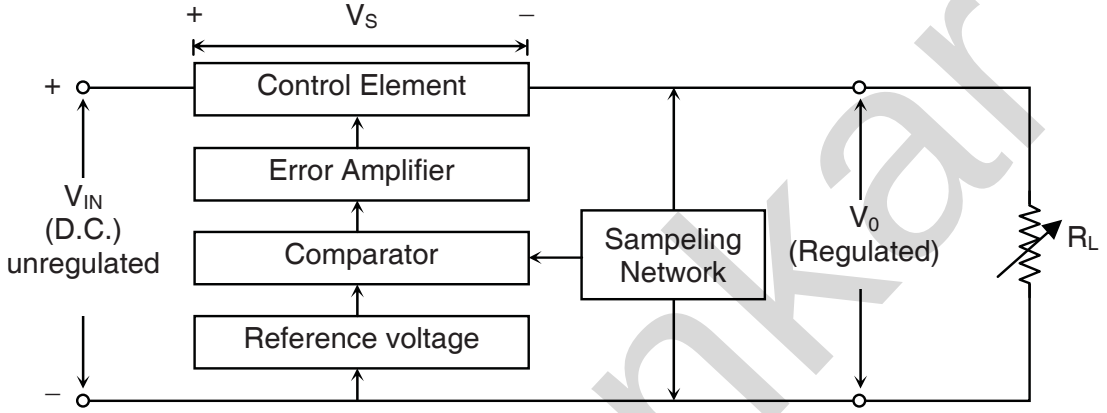
**(A) Comparison between 3 configurations of transistor**

| | Parameter | Common Base | Common Emitter | Common collector |
|---|---|---|---|---|
| 1) | Input impedance | Lowest ≈ 25Ω | Medium ≈ 1kΩ | Highest = $\beta_{D.C} \times R_E$ |
| 2) | Output Impedance | Highest ≈ 1MΩ | Medium ≈ 50k to 100kΩ | Lowest = $R_E/\beta_{D.C.}$ |
| 3) | Current gain | $\propto_{D.C} \leq 1$ lowest | $100 < \beta_{D.C.} < 500$ high | $(\beta_{D.C.} + 1)$ Highest |
| 4) | Voltage gain | High | Highest | Less than 1 lowest |
| 5) | Power gain | Moderate | Highest | Medium |
| 6) | Leakage current | $I_{CBO} = I_{CO}$ lowest 5μ A for Ge, 1μA for Si | $I_{CEO} = \beta_{D.C}.I_{CBO}$ High 500μA for Ge, 20μA for Si | $I_{CEO}$ High 500μA for Ge, 20μA for Si |
| 7) | Phase shift | 0° (In phase) | 180° (out of phase) | 0° (In phase) |
| 8) | Cut-off frequency | High | Lower than CB | Depends upon load |

| | | | | |
|---|---|---|---|---|
| 9) | Thermal stability | High | Low | High |
| 10) | Applications | For high frequency | For audio frequency | For impedance matching as a buffer. |

**Q.2(c) Draw the functional block diagram of controlled series voltage regulator and explain the functions of each block.** **[4]**

**(A) Controlled Series Voltage Regulator**




Important blocks and their functions are :

**i) Reference voltage :** Properly reverse biased zener diode is used as constant D.C. reference voltage.

**ii) Sampeling network :** Two resistors are connected as potential divider across the output terminals for sampeling the output voltage.

**iii) Comparator :** Op–amp or transistor compares the actual sampled output voltage with constant reference voltage. The difference between them known as error voltage is present at its output.

**iv) Error Amplifier :** It amplifies the error voltage given to it. This is now used as control voltage to adjust the voltage drop across control element. Normally in most of the circuit same transistor or same op–amp is used as both comparator and error amplifier.

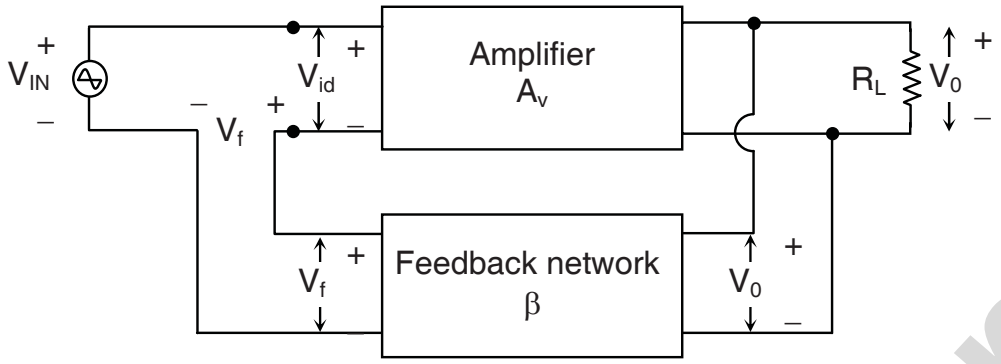
**v) Control element :** A transistor in active region is working as emitter follower. This transistor is working as a variable resistance. The voltage drop $V_S$ across it is automatically adjusted by control signal till error voltage becomes zero. Due to this $V_0$ is kept constant under all conditions.

**Q.2(d) State the types of –ve feedback amplifiers and draw their functional block diagrams. Also state the effect on $R_{IN}$ and $R_0$.** **[4]**

**(A)** There are 4 types of –ve feedback amplifier :

1) Voltage series
2) Voltage shunt
3) Current series
4) Current shunt

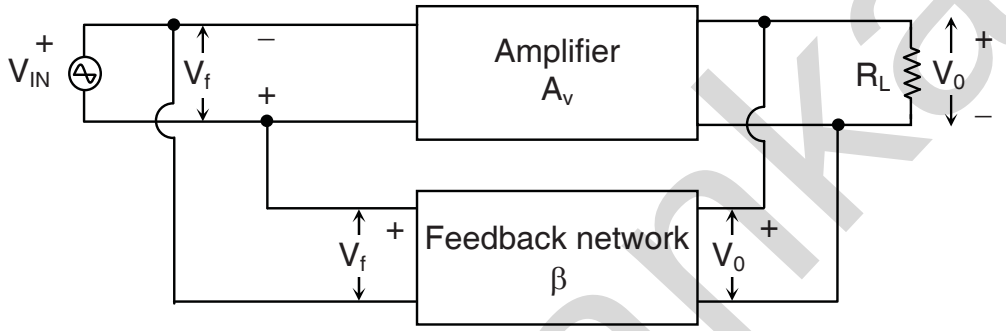
### 1) Voltage series –ve feedback amplifiers




(a) $R_{IN} \uparrow$
(b) R0 $\downarrow$

**Fig. (a)**

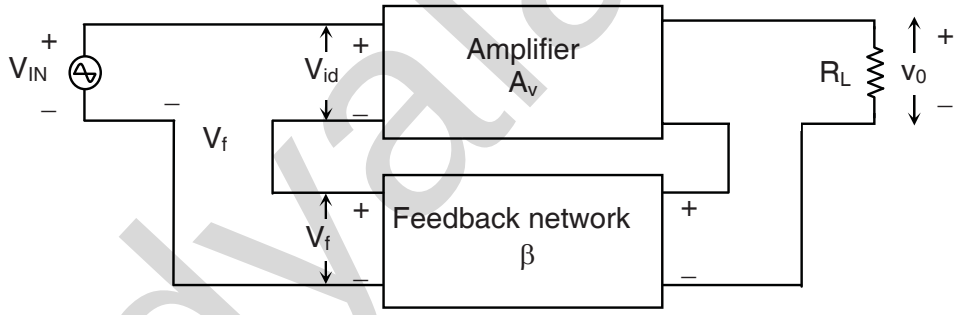
### 2) Voltage shunt




(a) $R_{IN} \downarrow$
(b) $R_0 \downarrow$

**Fig. (b)**

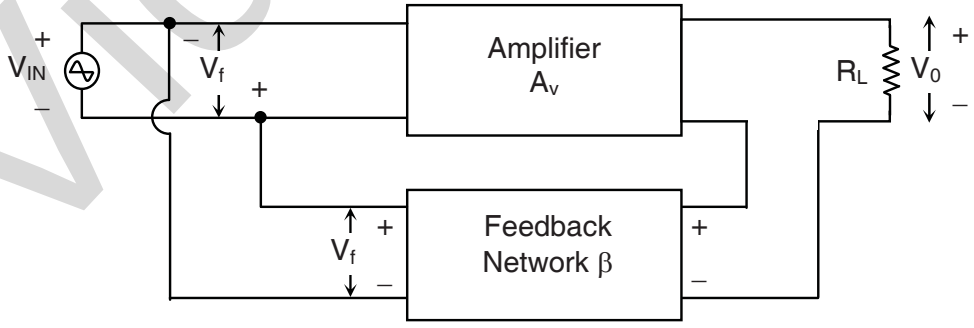
### 3) Current Series




(a) $R_{IN} \uparrow$
(b) $R_0 \uparrow$

**Fig. (c)**

### 4) Current Shunt




(a) $R_{IN} \downarrow$
(b) $R_0 \uparrow$

**Fig. (d)**

**Note :**

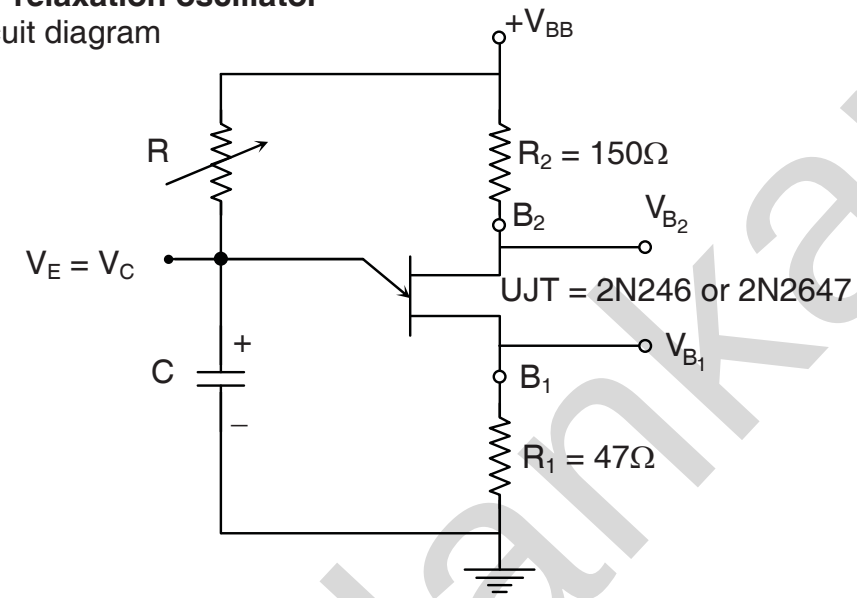
(i) An ammeter is connected in series while voltmeter is connected in parallel.
(ii) Hence at the output if it is parallel connection then it is voltage feedback and if it is series connection then it is current feedback.

(iii) Similarly at the input if it is series connection then it is series feedback and if it is parallel connection then it is shunt feedback.
(iv) If 2 resistors are connected in series then $R_S$ increases.
(v) If 2 resistors are connected in parallel then $R_P$ decreases.

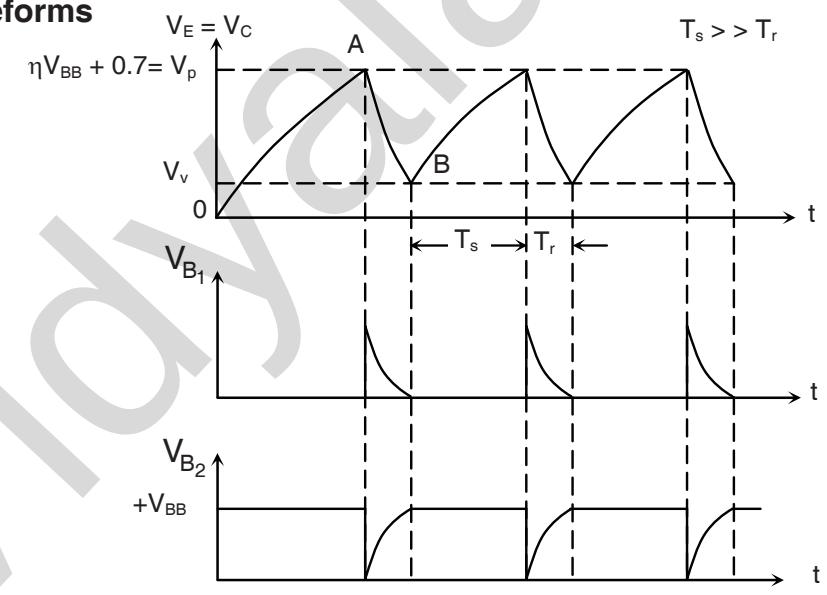
**Q.2(e) Draw UJT relaxation oscillator circuit and explain its working with the help of 3 waveforms.** **[4]**

**(A) (a) UJT relaxation oscillator**

Circuit diagram




**(b) Waveforms**




$V_{B_1}$ positive pulses are used for triggering S.C.R.

**Working :** At the start (t = 0) when d.c. supply of $V_{BB}$ volts is given to the circuit, there is no charge on capacitor and hence $V_C = V_E = 0$. This is anode of internal P – N junction which is at 0 volts. Due to internal potential divider of UJT, the cathode voltage $V_K$ of P-N junction is given by $V_k = \eta V_{BB}$ where $\eta$ = Intrinsic stand-off ration = 0.7. Since $V_A < V_k$, internal P-N junction is reverse biased and hence UJT remains off.

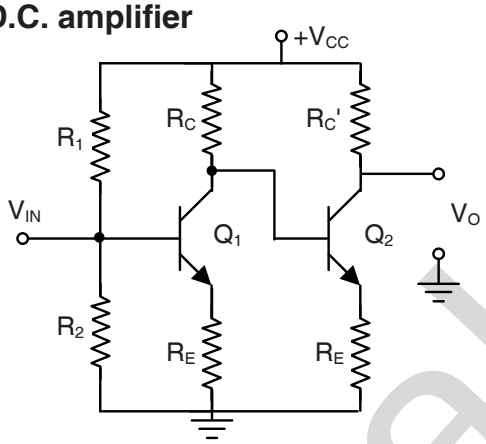
OFF UJT acts like open switch and allows capacitor C to charge towards $+V_{BB}$ through variable resistor R. $V_C = V_E$ now starts increasing exponentially and when $V_E = (\eta V_{BB} + 0.7) = V_P$ then internal P-N junction is forward biased and starts conducting. UJT is now switched on and the charged capacitor starts discharging through ON UJT and resistor $R_1$. $V_C = V_E$ starts decreasing exponentially and when $V_E = V_v$ valley voltage, UJT goes automatically off.

OFF UJT once again acts like open switch and allows capacitor to charge. The entire waveform (O-A-B) respects itself thus producing continuous periodic sweep voltage oscillations.

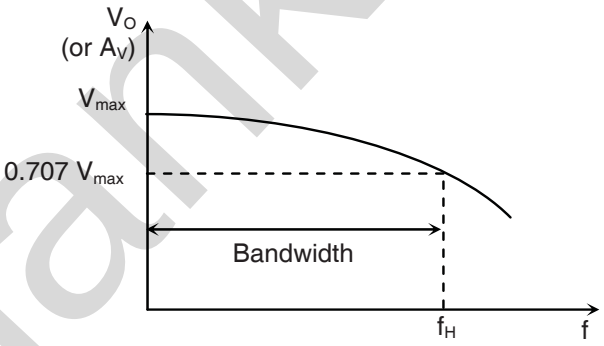
In the above circuit charging time constant = $R \times C$
While discharging time constant = $R_1 \times C$
Since $R >> R_1$, we get $T_s >> T_r$ which is the condition required for sweep voltage.

**Q.2(f) Draw the circuit diagram of direct coupled amplifier and explain its working.** **[4]**

**(A) D.C. amplifier**




Frequency response




To improve the low frequency response, all the capacitors in the circuit are removed. Hence output of 1st stage (i.e., collector of $TR_1$) is directly connected to the base of $TR_2$. No coupling network is used and hence it is known as direct coupled amplifier.

This is the only amplifier capable of amplifying very low f A.C. signal as well as D.C. signal of zero frequency and hence it is called A.C. amplifier. Though it is mainly used for amplifying D.C. signal of zero frequency, it is also used for amplifying A.C. signal upto $f_H$ which is sufficiently high compared to audio frequency of 20 kHz.

**Q.3 Attempt any FOUR of the following :** **[16]**

**Q.3(a) Give comparison between voltage amplifier and power amplifier.** **[4]**

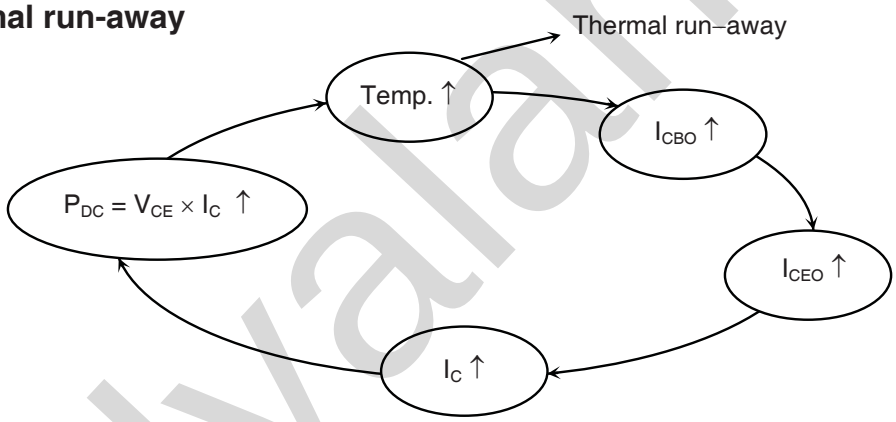
**(A) Comparison between voltage amplifier and power amplifier**

| | Voltage Amplifier | Power Amplifier |
|---|---|---|
| 1) | Amplifies voltage & voltage gain. $Av = \frac{V_O}{V_{IN}}$ | Amplifies power & power gain. $A_p = \frac{P_0}{P_{IN}}$ |
| 2) | Small signal amplifier. $V_{IN}$ in mV. | Large signal amplifier. $V_{IN}$ in volts. |
| 3) | Class A amplifier. | Class B or Class C amplifier. |
| 4) | Distortion low. | Distortion high. |

| | | |
|---|---|---|
| 5) | Physical size of transistor used is small and has plastic package. | Physical size of transistor used is large and has metal package. |
| 6) | $\beta_{D.C.} > 100$ | $20 \leq \beta_{D.C} \leq 50$ |
| 7) | Collector current 1 to 5 mA. | $I_C > 100$ mA |
| 8) | A.C. output power is low in mW. | $P_{AC} > 1$ watt |
| 9) | Output impedance is high ≈10 kΩ to 12kΩ | Output impedance low ≈ 200Ω |
| 10) | Normally R–C coupled. | Normally transformer coupled or direct coupled. |
| 11) | Heat sinks not required. | Heat sinks must be used with power transistor. |
| 12) | Impedance matching poor. | Excellent impedance matching. |
| 13) | Transistor used BC 147, 148, 547, 548. 549. | Power transistor used SL100–SK100, AC187–AC188, 2N3055. |
| 14) | Transistors have thin base since it handles low current. | It has thick base to handle large current. |

**Q.3(b) Write a note on "Thermal run–away" in transistor. Why is showed be avoided.** **[4]**

**(A) Thermal run-away**




i) $P_{D.C.} = V_{CE} \times I_C$

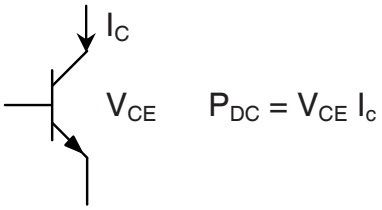
ii) Temp. $\propto P_{D.C.}$

iii) $I_{CBO} \propto$ Temp.

iv) $I_{CEO} \approx 100\ I_{CBO}$

v) $I_C = \beta I_B + I_{CEO}$

When D.C. voltage is applied to transistor, collector current $I_C$ starts flowing. This produces voltage drop $V_{CE}$ on the transistor.




Due to this D.C. power is dissipated in Transistor and its temperature increases. This increases $I_{CBO}$ and since $I_{CEO} = 100\ I_{CBO}$ and $I_C = \beta_{D.C.}\ I_B + I_{CEO}$, both $I_{CEO}$ and $I_C$ increase. This again increases $P_{D.C.}$ and temperature of transistor. This is a closed cycle due to which temperature of transistor continuously goes on increasing.

"The damaging of a transistor due to continuous rise in its temperature is defined as the thermal run–away".

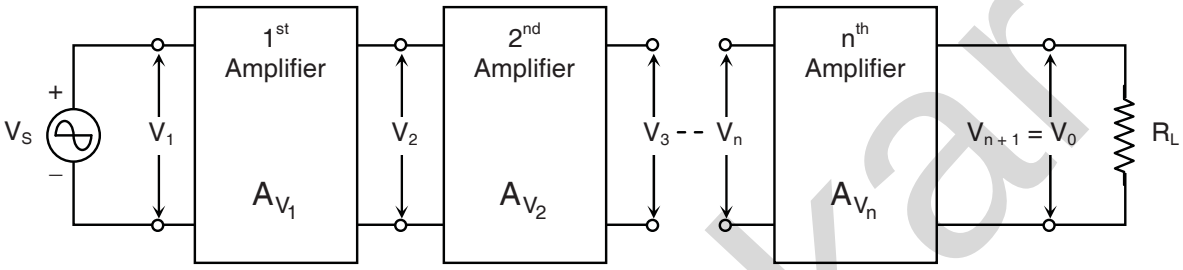
It can be avoided by

(i) Selecting proper transistor biasing circuit.

(ii) By using transistor biasing stabilization circuits.

**Q.3(c) Draw the block diagram of multi-stage amplifier and derive an expression for its overall voltage gain.** **[4]**

**(A) Multi-stage amplifier**




Let $A_{V_1}, A_{V_2}, \ldots\ldots, A_{V_n}$ be the voltage gains of each amplifier connected in cascade. A.C. input voltage $V_S$ to be amplified is given to the input terminals of 1st amplifier. The output voltage $V_O$ is taken across $R_L$ connected to the output terminals of nth amplifier. By definition of voltage gain, we have

$$A_V = \frac{\text{output voltage}}{\text{input voltage}}$$

Hence, $A_{V_1} = \frac{V_2}{V_1}; A_{V_2} = \frac{V_3}{V_2}; A_{V_3} = \frac{V_4}{V_3}; \ldots\ldots; A_{V_{n-1}} = \frac{V_n}{V_{n-1}}; A_{V_n} = \frac{V_{n+1}}{V_n}$ and over-all voltage gain $A_V = \frac{V_O}{V_S}$. Multiplying individual voltage gains of each amplifier, we get

$$A_{V_1} \times A_{V_2} \times A_{V_3} \times \ldots\ldots \times A_{V_{n-1}} \times A_{V_n} = \frac{V_2}{V_1} \times \frac{V_3}{V_2} \times \frac{V_4}{V_3} \times \ldots\ldots \times \frac{V_{n-1}}{V_{n-1}} \times \frac{V_n}{V_{n-1}} \times \frac{V_{n+1}}{V_n}$$

$$= \frac{V_{n+1}}{V_1} \quad \text{But } V_{n+1} = V_O \text{ and } V_1 = V_S$$

$$= \frac{V_O}{V_S} = A_V$$

Hence $A_V = A_{V_1} \times A_{V_2} \times A_{V_3} \times \ldots\ldots \times A_{V_n}$.

Hence overall voltage gain $A_V$ of multi-stage amplifier is obtained by multiplying the voltage gains of individual amplifiers connected in cascade.

**Q.3(d) Define the following characteristics of regulated power supply : (i) Voltage regulation or Load regulation, (ii) Line regulation, (iii) Ripple rejection and (iv) Output impedance.** **[4]**

**(A) (i) Voltage regulation or Load regulation**

Let $V_{NL}$ = output D.C. voltage at no load (open circuit)

$V_{FL}$ = output D.C. voltage when full rated load current is flowing

Then % of V.R. = % of L.R. = $\left(\frac{V_{N.L.} - V_{F.L.}}{V_{F.L.}}\right) \times 100$

It is defined as the ratio of change in D.C. output voltage when load current changes from 0 to full rated load, to the D.C. output voltage at full load.

Ideally its value should be zero and practically it must be as low as possible.
(**Note :** Since the change in $V_0$ is produced due to change in load current, it is known as voltage regulation or load regulation).

**(ii) Line (source) regulation**

Let $V_{HL}$ = Load (output) D.C. voltage with high line (A.C.) voltage
$V_{LL}$ = Load (output) D.C. voltage with low line voltage
$V_N$ = Normal D.C. output voltage.

Then, % of S.R. = $\left(\frac{V_{H.L.} - V_{N.L.}}{V_N}\right) \times 100$

It is defined as the change in output D.C. voltage to the change in A.C. input voltage and is expressed in mV or percentage of output voltage.
Ideally it should be zero and practically as low as possible.

**(iii) Ripple Rejection**

It denotes the regulators ability to reject unwanted ripple voltage. It is normally expressed in dB.

Ripple rejection in dB = $20 \log_{10}\left(\frac{V_{ripple(output)}}{V_{ripple(input)}}\right)$

It is defined as 20 times the common logarithm of voltage ratio obtained by dividing A.C. ripple voltage at the output of regulator to the A.C. ripple voltage at the input of regulator.
Ideally it should be zero and practically as small as possible.

**(iv) Output impedance ($Z_0$)**

$$Z_0 = \frac{\Delta V_0}{\Delta I_L}$$

It is defined as the ratio of incremental change in output D.C. voltage $\Delta V_0$, to the incremental change in output load current $\Delta I_L$. It is measured in ohms. $Z_0$ should be as small as possible. Since when $I_L$ flows through it a voltage drop $I_L$ $Z_0$ is produced on it. The final D.C. output voltage reduces by this amount which should be ideally zero (i.e., $Z_0 = 0$)

$Z_0$ can be reduced by
1) Using transistor as emitter follower.
2) Using –ve feedback in the circuit

**Q.3(e) Define sweep speed for a sweep waveform. Name and define the errors which are present in sweep signal. [4]**

**(A)** Sweep speed = $\frac{dv_c}{dt}$ i.e. it is defined as the rate of change of sweep voltage w.r.t. time. For sweep voltage to be linear then sweep speed must be constant. For this constant current charging of capacitor is used

where $v_c = \frac{1}{C}\int i\,dt = \frac{I}{C}\int dt$

$\therefore \quad v_c = \frac{It}{C}$

$\therefore \quad \frac{dv_c}{dt} = \frac{I}{C} = \text{constant}$

There are 3 types of errors which can be present in a sweep voltage.

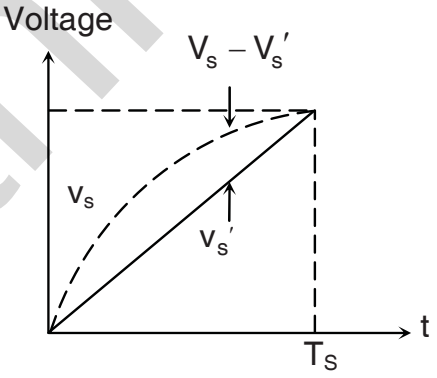
1) Slope or sweep speed error ($e_s$)
2) Displacement error ($e_d$)
3) Transmission error ($e_t$)

1) The slope or sweep speed error ($e_s$)

$$e_s = \frac{\text{Difference in slope at beginning and end of sweep}}{\text{Initial value of slope}}$$

For ideal linear sweep, the slope remains same because it is a straight line and hence $e_s = 0$ for ideal sweep.

2) The displacement error ($e_d$)




$v_s$ = Instantaneous value of actual sweep voltage

$v_s'$ = Instantaneous value of linear sweep voltage

$V_s$ = Maximum value of actual sweep voltage

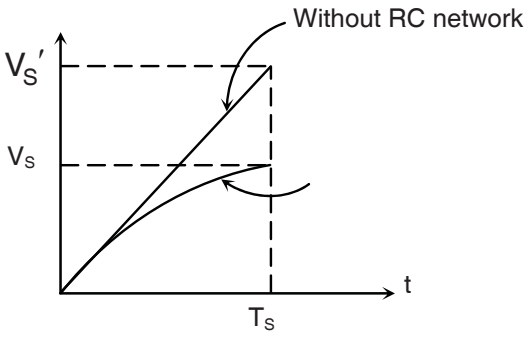
Then $e_d = \frac{(v_s - v_s')_{max}}{V_s}$. Thus it is defined as the ratio of maximum difference between the actual sweep voltage and the linear sweep voltage to the maximum value of actual sweep voltage.

3) The transmission error ($e_t$)

$V_S$ = Actual sweep voltage

$V_s'$ = Linear sweep voltage

Normally R–C coupling network is used at the output due to which transmission error is introduced.




Transmission error $e_t = \frac{V_s' - V_s}{V_s'}$

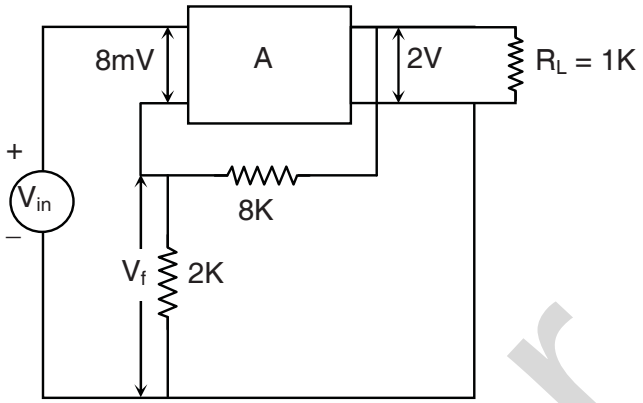
It is defined as the ratio of difference between uncompensated output and compensated output to the uncompensated output.

**Q.3(f) A feedback amplifier is shown in figure calculate :** **[4]**

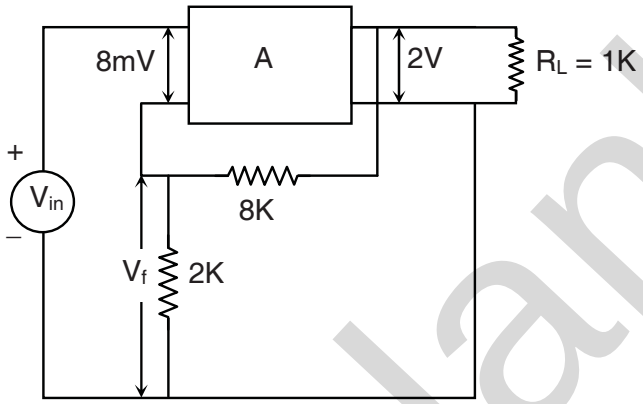
**(i) Value of feedback factor**

**(ii) Voltage gain A of amplifier without feedback**

**(iii) The feedback voltage $V_f$.**

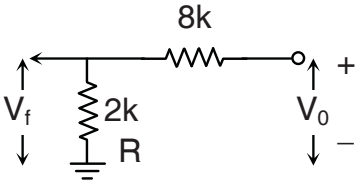



**(A)**




(a) By potential divider formula

$$V_f = \left(\frac{R_1}{R_1+R_2}\right)\times V_0 = \left(\frac{2}{2+8}\right)\times V_0$$




$\therefore V_f = 0.2\ V_0$ …(1)

$= 0.2 \times 2 = 0.4$ volts $[\because V_0 = 2V]$

$\therefore V_f = 0.4$ volts

(b) From equation (1) $V_f = 0.2\ V_0$ But $V_f = \beta\ V_0$

Hence feedback factor $\beta = 0.2$

(c) $A = \frac{V_0}{V_{id}}$ where $V_0 = 2 \times 10^3$ mV and $V_{id} = 8$ mV

$\therefore$ Open loop gain, $A = \frac{2\times10^3}{8} = 250 = A$

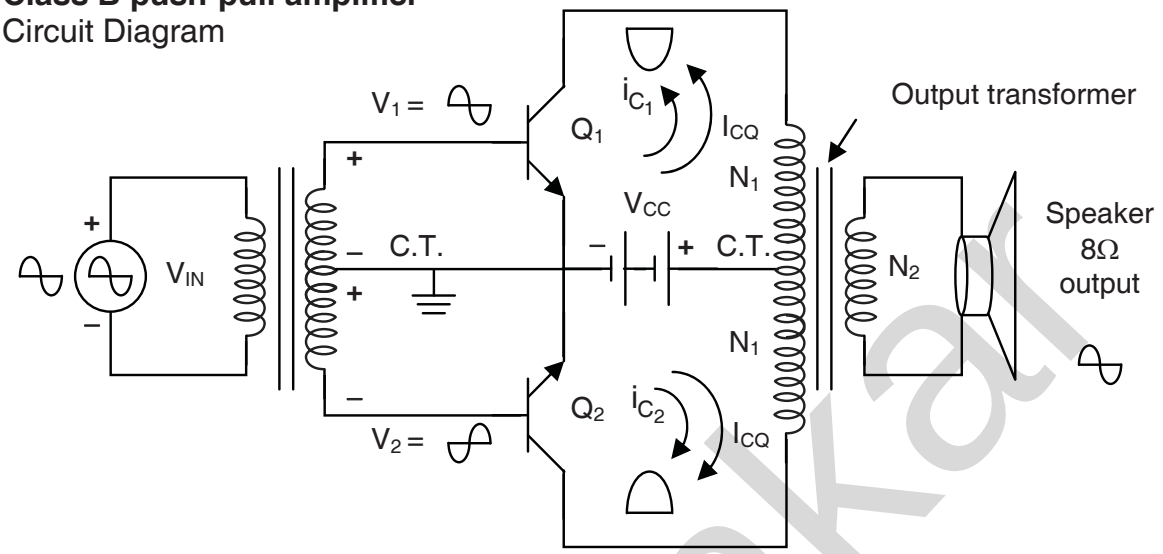
(d) $A_{fb} = \frac{A}{1+A\beta} = \frac{250}{1+250\times0.2} = \frac{250}{51} = 4.902$

**Q.4 Attempt any FOUR of the following : [16]**

**Q.4(a) Draw the circuit diagram of Class B push-pull amplifier and explain its working. [4]**

**(A) Class B push-pull amplifier**

Circuit Diagram




**Working :** The two NPN power transistors are connected in push-pull, i.e., when one transistor is ON the other is OFF and vice-versa. Emitters of both transistors are connected to ground while base of both transistors is connected to ground through centre tap secondary of driver transformer. A.C. input voltage $V_{IN}$ to be amplified is given to the primary of driver transformer. Its centre-tapped secondary is used for producing two equal and opposite signals $V_1$ and $V_2$ which are given to the base of both transistors. Similarly, collectors of both transsitor are connected to the primary of output transformer. A $+V_{CC}$ D.C. supply is given to the centre top of primary. Speaker of 8Ω is connected to the secondary of output transformer. The turns ratio $N_1 : N_2$ is adjusted for proper impedance matching.

$$R'_L = \left(\frac{N_1}{N_2}\right)^2 \times R_L \quad [R_L = 8\Omega]$$

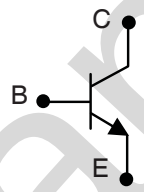
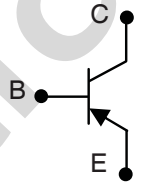
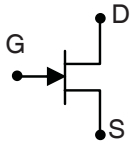
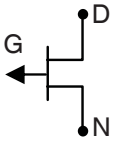
When A.C. input signal $V_{IN}$ is not given then both $Q_1$ and $Q_2$ are in cut-off because base and emitter of transistors is at O D.C. volts. As shown above $V_1$ is in phase with and $V_2$ is output of phase with A.C. input signal $V_{IN}$. For the first +ve half cycle of $V_{IN}$, the –ve half cycle of $V_2$ drives $Q_2$ more into cut-off while +ve half cycle of $V_1$ drives $Q_1$ into conduction when $V_1$ becomes + 0.7 volts. Similarly for the next half cycle $Q_2$ conducts and $Q_1$ is driven into cut-off.

$Q_1$ thus produces 1st half cycle while $Q_2$ produces 2nd half cycle. These are transferred to speaker by output transformer and hence both the half cycles are produced at the output, thus reducing distortion.

**Q.4(b) Give the comparison between BJT and JFET. [4]**

**(A) Comparison between BJT and JFET**

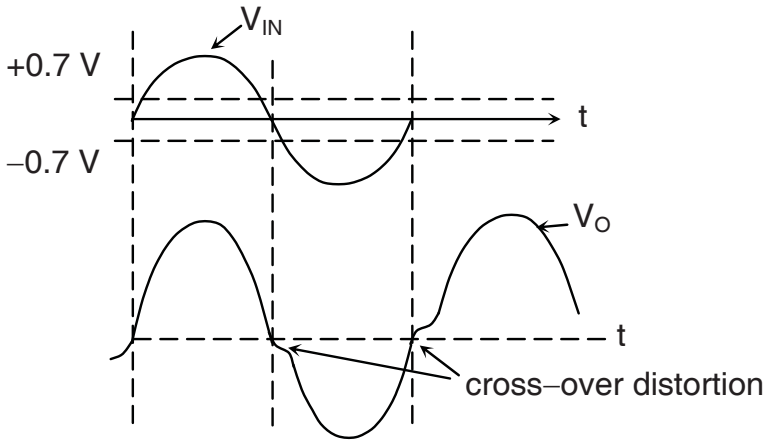
| | Parameter | BJT | FET |
|---|---|---|---|
| 1) | Control Element | Current controlled device input current $I_B$ controls output current $I_C$ | Voltage controlled device. Input voltage $V_{GS}$ controls output current $I_D$. |

| | | | |
|---|---|---|---|
| 2) | Device type | Bipolar : Current flow due to both majority and minority carriers | Unipolar : Current flow due to majority carriers only |
| 3) | Input junction | B–E junction is forward biased | G–S junction is reverse biased. |
| 4) | Input resistance | Very low compared to JFET of the order of few KΩ. | Very high of the order of several MΩ. |
| 5) | Thermal stability | Less hence thermal run-away possible. | More hence thermal run–away not present |
| 6) | Thermal Noise | More noisy | Less noisy |
| 7) | Gain–Bandwidth product | High | Low |
| 8) | Switching speeds | High | Low |
| 9) | Cut–off frequency | Low | High |
| 10) | Size | Bigger than JFET less suitable for I.C. fabrication | Smaller and hence more suitable for I.C. fabrication. |
| 11) | Type and symbols | (a) N – P – N   (b) P – N – P   | (a) N – Channel   (b) P– Channel   |
| 12) | Application | Low frequency amplifiers and oscillators | (1) High f application (2) Impedance matching to avoid loading effect |

**Q.4(c) Write a note on cross–over distortion. [4]**

**(A) CROSS–OVER DISTORTION**

For class B operation base and emitter of power transistors are kept at 0 volt D.C. Hence when A.C. input signal are not given both the transistors are in cut off region.



A silicon transistor requires + 0.7 V (for NPN transistor) and –0.7 V (PNP transistor) w.r.t. emitter to conduct. Due to this only when a.c. input signal reaches ± 0.7 V, then only the two transistors start conducting. As shown above, when $V_{IN} \leq \pm$ 0.7V, then two transistors do not conduct resulting in the distortion of output signal. This distortion occurs whenever A.C. signal is crossing from +ve to –ve or –ve to +ve cycle and hence it is known as cross–over distortion.
This can be avoided by using class AB power amplifier. Q point is selected slightly in active region due to which transistor conducts for slightly more than half cycle thus avoiding cross–over distortion.

**Q.4(d) Find 'f' for UJT relaxation oscillator if R = 10k, C = 0.1μF. Assume suitable value for η.** [4]

**(A)** Since $\eta < 1$. Normally $\eta = 0.7$

$R = 10\ k = 10 \times 10^3\ \Omega$ and $C = 0.1 \times 10^{-6}\ F$

By formula $T = RC \log_e \left(\frac{1}{1-\eta}\right)$

Now $\frac{1}{1-\eta} = \frac{1}{1-0.7} = \frac{1}{0.3} = 3.33$

Hence $\log_e(3.33) = 1.203$

$\therefore \quad T = 10 \times 10^3 \times 0.1 \times 10^{-6} \times 1.203 = 1.203 \times 10^{-3}$ sec

$f = \frac{1}{T} = \frac{1}{1.203 \times 10^{-3}} = \frac{10^3}{1.202} = \frac{1000}{1.202}$

$\therefore \quad f = 831.95$ Hz

**Q.4(e) Prove that reverse leakage current in common emitter is 100 times more than the reverse leakage current of common base configuration. i.e. prove that $I_{CEO} = 100\ I_{CBO}$.** [4]

**(A)** For common emitter configuration
The exact relation between output current $I_C$ and input current $I_B$ is given by

$I_C = \beta_{DC}\ I_B + I_{CEO}$ …(i)

Similarly for common base configuration
The exact relation between output current $I_C$ and input current $I_E$ is given by

$I_C = \alpha_{D.C.}\ I_E + I_{CO}$ [$I_{CO}$ or $I_{CBO}$]

Now put $I_E = I_C + I_B$

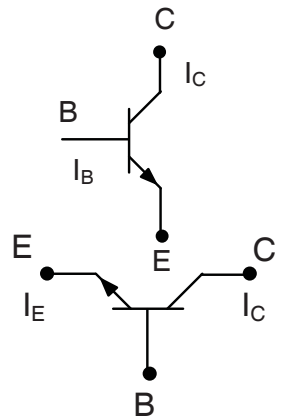
$\therefore \quad I_C = \alpha_{D.C.}\ (I_C + I_B) + I_{CO}$

$= \alpha_{D.C.} I_C + \alpha_{D.C.} I_B + I_{CO}$

$\therefore \quad I_C - \alpha_{D.C.} I_C = \alpha_{D.C.} I_B + I_{CO}$

$\therefore \quad (1 - \alpha_{D.C.}) I_C = \alpha_{D.C.} I_B + I_{CO}$

$\therefore \quad I_C \left(\frac{\alpha}{1-\alpha}\right) I_B + \frac{I_{CO}}{1-\alpha}$ …(ii)




Companies equations (i) & (ii) we get

$\beta = \frac{\alpha}{1-\alpha}$ and $I_{CEO} = \left(\frac{1}{1-\alpha}\right) I_{CO}$

Now by formula $\alpha = \frac{\beta}{\beta+1}$

$$\therefore \quad I_{CEO} = \left(\frac{1}{1-\frac{\beta}{\beta+1}}\right) I_{CO} = \left(\frac{1}{\frac{\beta+1-\beta}{\beta+1}}\right) I_{CO} = (\beta+1) I_{CO}$$

But normally $100 < \beta < 500$. Also neglecting 1 we can write $\beta + 1 \approx 100$

$\therefore$ $I_{CEO} = 100\ I_{CO}$

Hence reverse leakage current in common emitter is 100 times greater than the reverse leakage current in common base configuration.

**Q.4(f) Explain the working of RC phase shift oscillator. [4]**

**(A) RC Phase Shift Oscillator using Transistor**

- A typical RC phase shift oscillator using transistor as an active device is shown in figure 1.
- The Circuit consists of a single stage amplifier in C.E. configuration and the RC phase shifting network.
- The resistors $R_1$, $R_2$ and $R_E$ are connected for transistor biasing CE is the emitter bypass capacitor.

**Operation :**

- As shown in figure 1 the output $V_o$ of the single stage CE amplifier has been connected as an input to the RC phase shifting network.
- The output of the phase shifting network is connected at the input of the amplifier.
- As the amplifier is C.E. type, it introduces a phase shift of 180° between its input and output. The phase shifting network will introduce an additional 180° phase shift to make the phase shift around the loop equal to zero.

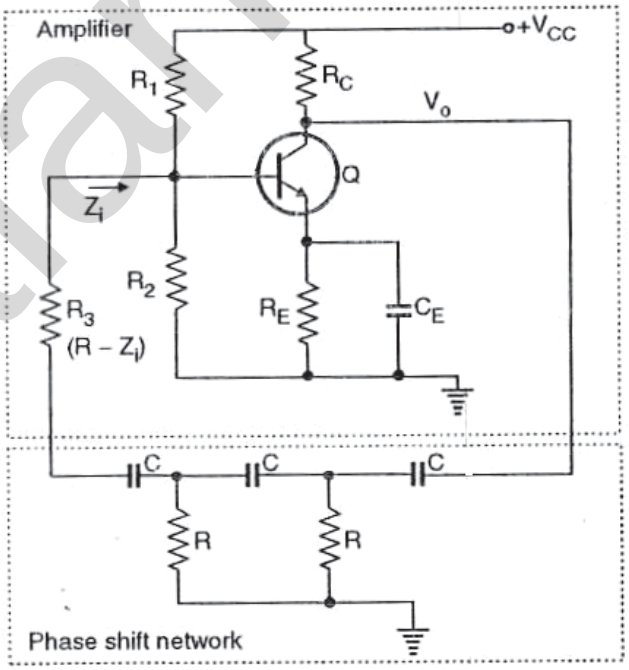



**Fig. 1 :** RC phase shift oscillator using transistor

- The phase shift around the loop will be precisely equal to 0° only at one frequency "f" which is the frequency of operation. If the gain of the amplifier and feedback factor $\beta$ are adjusted properly to have a loop gain $|A\beta| \geq 1$ the sustained sinusoidal oscillations will be obtained at the oscillator output.
- Note that the RC feedback network of figure 1 is slightly different from the one we have discussed in section 6. The resistance $R_3$ of Figure 1 is selected in such a way that,

$$R_3 + Z_i = R \qquad \ldots (1)$$

where, $Z_i$ = Input impedance of the CE amplifier. It is given by,

$Z_i = h_{ie} \parallel (R_1 \parallel R_2)$

- But as $R_1$ and $R_2$ are large enough. We can neglect them. Hence,
  $Z_i \approx h_{ie}$
- Substituting this value into Equation (1) we get,
  $R_3 + h_{ie} = R$ or
  $R_3 = R - h_{ie}$ ... (2)
- And if we do not neglect the resistors $R_1$ and $R_2$ then the value of $R_3$ is given by,
  $R_3 = R - [R_1 \parallel R_2 \parallel h_{ie}]$ ... (3)

**Q.5 Attempt any FOUR of the following : [16]**

**Q.5(a) Explain why stability of the amplifies improves when –ve feedback is used. [4]**

**(A)** $A_v$ = open loop voltage gain;
$A_{fb}$ = Closed loop voltage gain;

$\beta$ = feedback factor then by formula $A_{fb} = \dfrac{A_v}{1 + A_v\beta}$

Now $\beta \leq 1$ i.e. normally $\beta$ is always less than 1 and its maximum value can be only one. But the open loop voltage gain $A_v$ is very high and hence $A_v\beta >> 1$. Neglecting 1 in the denominator we get

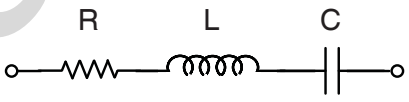
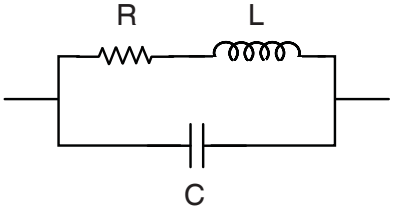
$$A_{fb} = \frac{A_v}{A_v\beta} = \frac{1}{\beta}$$

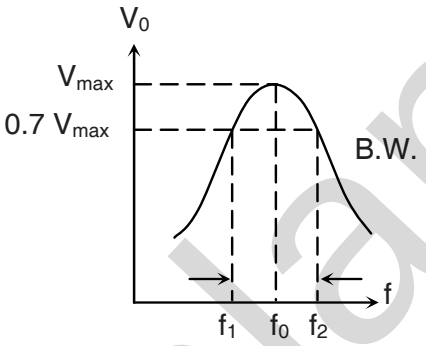
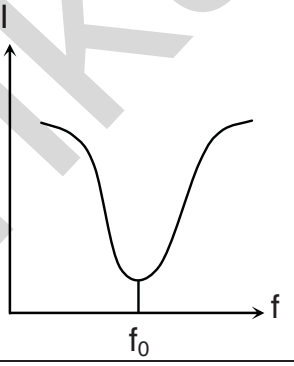
Thus closed loop gain $A_{fb}$ is equal to the reciprocal of feedback factor $\beta$.
In –ve feedback amplifiers only resistors are used whose values are fixed once they are selected. $\beta$ = Ratio of these resistors $\left(\beta = \dfrac{R_1}{R_1 + R_f}\right)$ which is constant.

Thus $A_{fb}$ remains constant and is independent of the parameter of the transistor ($\beta_{a.c}$ or $h_{fe}$). Because of this reason, stability of voltage amplifier improves when –ve feedback is used.

**Q.5(b) Give the comparison between series and parallel resonant circuit. [4]**

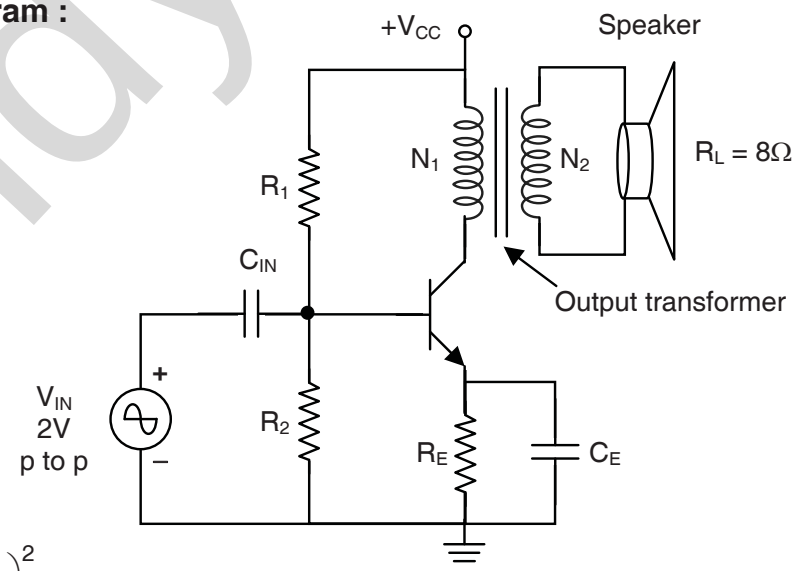
**Q.5(b) Comparison between series and parallel resonant circuit**

| | Parameter | Series Resonant Circuit | Parallel Resonant Circuit |
|---|---|---|---|
| 1) | Circuit |  i.e. R, L and C are in series. |  i.e. coil and C are in parallel. |
| 2) | $f_0$ | $f_0 = \dfrac{1}{2\pi\sqrt{LC}}$ | $f_0 = \dfrac{1}{2\pi}\sqrt{\dfrac{1}{LC} - \dfrac{R^2}{4L^2}} \approx \dfrac{1}{2\pi\sqrt{LC}}$ where $R \approx 0$ and can be neglected. |
| 3) | $\phi$ | Phase angle $\phi = 0$ i.e. 'I' and $V_{in}$ are in phase at $f_0$. | Phase angle $\phi = 0$ at $f_0$. |
| 4) | p.f. | p.f. = cos $\phi$ = 1 | p.f. = cos $\phi$ = 1 |

| | Parameter | Series Resonant Circuit | Parallel Resonant Circuit |
|---|---|---|---|
| 5) | Reactance | $X_L = X_C$ at $f_0$<br>X = reactance | $B_L = B_C$ at $f_0$<br>B = Susceptance |
| 6) | $Z_{eff}$ | $Z_{eff}$ = R and is minimum | $Z_{eff} = \frac{L}{RC}$ and is maximum |
| 7) | $I_0$ | max. at $f_0$ and $I_0 = \frac{V_{IN}}{R}$ | $I_0 = \frac{V_{IN}}{L/RC} = \frac{RCV_{IN}}{L}$<br>and is minimum |
| 8) | $Q_0$ | $Q_0 = \frac{\omega_0 L}{R} = \frac{1}{\omega_0 RC} = \frac{1}{R}\sqrt{\frac{L}{C}}$<br>and is known as voltage magnification factor | $Q_0 = \frac{\omega_0 L}{R} = \frac{1}{\omega_0 RC} = \frac{1}{R}\sqrt{\frac{L}{C}}$<br>and is known as current magnification factor. |
| 9) | | At $f_0$, $V_L = V_C = Q_0 V_{IN}$ i.e. i.e. $V_L$ and $V_C$ are more than $V_{IN}$. | At $f_0$, $I_C = Q_0 I_T$ i.e. $I_C$ is more than $I_T$. |
| 10) | Resonance Curve |  |  |
| 11) | | B.W. = $\frac{f_0}{Q_0}$ | B.W. = $\frac{f_0}{Q_0}$ |

**Q.5(c) Draw the circuit diagram of single ended or transformer coupled class A amplifier and explain its working.** **[4]**

**(A) Circuit diagram :**




$R'_L = \left(\frac{N_1}{N_2}\right)^2 \times R_L$ where $R'_L$ is the impedance transferred to primary side.

**Working :** The resistors $R_1$ and $R_2$ are voltage divider biasing network which establishes Q point in the centre of a active region. $R_E$ stabilizes the Q point. By-pass capacitor $C_E$ by-passes A.C. output signal from the emitter. This removes –ve feedback which improves the gain of the amplifier. Input capacitor $C_{IN}$ blocks D.C. voltage and allows A.C. input voltage $V_{IN}$ to pass to the base of transistor.

The collector resistor $R_C$ is replaced by the primary winding of output transformer. Its resistance is very small which reduces power losses in it thus improving power efficiency. The maximum $\eta$ improves from 25% (for $R_C$) to 50% (for transformer coupled).

The transformer gives good D.C. isolation as well as impedance matching. Speaker impedance of 8Ω ($R_L$) on secondary side is transferred to $R'_L$ on primary side, where $R'_L = \left(\frac{N_1}{N_2}\right)^2 \times R_L$. Hence by using step-down ($N_2 < N_1$) transformers, impedance of speaker is matched to the output impedance of amplifier. Due to this maximum power is transferred to the loud-speaker.

**Q.5(d) (A) State the advantages and disadvantages of –ve feedback amplifier. [4]**

**Advantages :**

(i) Bandwidth of the amplifier increases $(B.W.)_{new} = (1 + A_v\beta)(B.W.)_{old}$

(ii) (Amplitude, frequency, phase harmonic) distortion of the amplifier reduces.

$$D_{0\,(new)} = \frac{D_{old}}{(1+A_v\beta)}$$

(iii) Noise signal in the output reduces.

$$N_{0(new)} = \frac{N_{0(old)}}{1+A_v\beta}$$

(iv) Stability of the amplifier improves due to which voltage gain becomes independent of transistor parameters and hence it remains almost constant.

(v) (a) $R_{IN}$ for voltage amplifier should be high.
(b) $R_0$ of voltage amplifier should be low.

By using voltage series –ve feedback amplifier, $R_{IN}$ increases and $R_0$ decreases.

$$R_{IN_{(new)}} = (1 + A_v\beta)\, R_{IN(old)}$$

$$R_{O(new)} = \frac{R_{0(old)}}{1+A_v\beta}$$

**Disadvantages :**

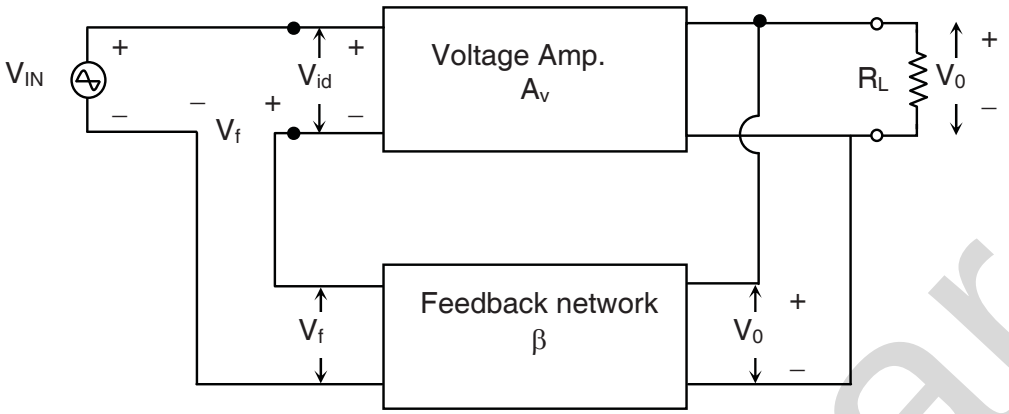
The only disadvantage is that voltage gain of the amplifier decreases

$$A_{fb} = \frac{A_v}{1+A_v\beta}$$

But if more voltage gain is required then multistage amplifiers with –ve feedback can be used.

**Q.5(e) Derive an expression for the closed loop gain of –ve feedback amplifier.** **[4]**

**(A)**




Applying K.V.L. at the input of the amplifier

We get $\sum$ All voltages = 0

$\therefore$ $+V_{IN} - v_{id} - v_f = 0$

$\therefore$ $V_{IN} - V_f = v_{id}$.

By definition of feedback factor $\beta = \frac{V_f}{V_0}$ hence $V_f = \beta v_0$. Putting this value in above equation we get

$$V_{IN} - \beta v_0 = v_{id} \qquad \ldots(1)$$

By definition of open loop voltage gain $A_V = \frac{v_0}{v_{id}}$

$\therefore$ $v_0 = A_V v_{id}$ from equation (1)

$v_0 = A_V (v_{IN} - \beta v_0)$

$= A_V v_{IN} - A_V \beta v_0$

$\therefore$ $V_0 + A_V \beta v_0 = A_v v_{IN}$

$\therefore$ $V_0 (1 + A_v \beta) = A_v v_{IN}$

$\therefore$ $$\frac{v_0}{V_{IN}} = \frac{A_V}{1 + A_V \beta}$$

But by definition $\frac{v_0}{V_{IN}} = A_{fb} =$ closed loop voltage gain.

Hence $$A_{fb} = \frac{A_v}{1 + A_v \beta}$$

In the above expression denominator > 1.

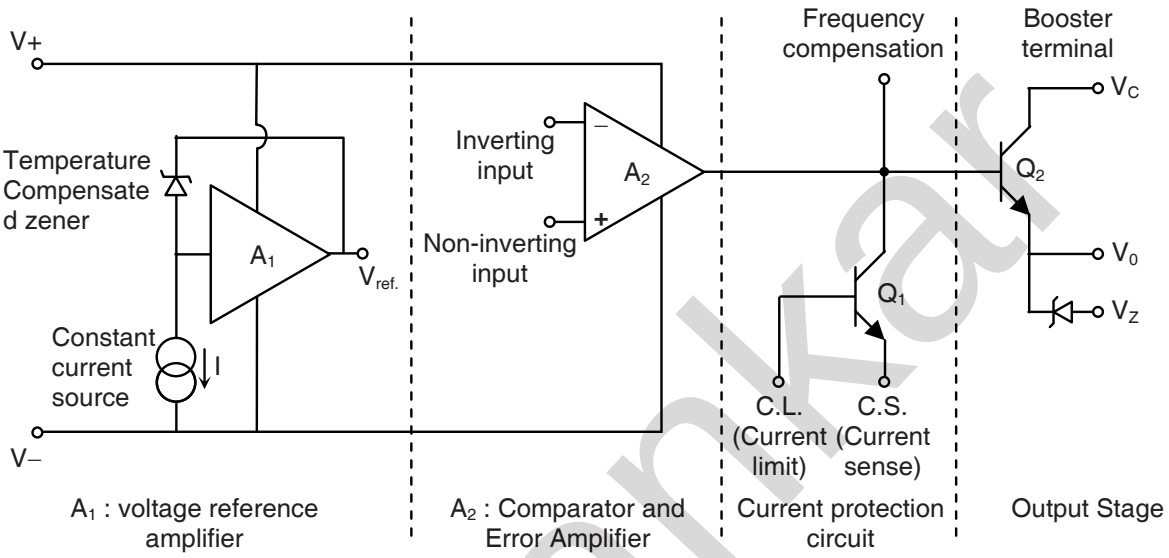
Hence $A_{fb} < A_v$ i.e. voltage gain of the amplifier reduces when –ve feedback is used.

**Q.5(f) Draw functional block diagram of I.C. 723 and explain it.** **[4]**

**(A)** I.C. 723 is basically a series voltage regulator. Its important blocks and their brief description is given below :

**i) Voltage Reference Amplifier :** A temperature compensated 6.2 V zener is biased with a constant current source. An op-amp $A_1$ is used as a buffer amplifier which provides reference output voltage of 7.15 V which is capable of supplying current upto 15 mA.

**ii) Comparator and error amplifier :** Op-amp $A_2$ is working both as comparator and error amplifier. The reference output (or fraction of it) is given to the non-inverting input terminal. Similarly the output voltage $V_0$ (or fraction of it) is given to the inverting input terminal of op-amp $A_2$. These two voltages are compared with each other and the difference between them known as error voltage is produced. This error voltage is amplified by op-amp $A_2$ and is available at its output as control voltage.




**iii) Output Stage :** It consists of series pass control transistor $Q_2$. The control voltage at the output of op-amp. $A_2$ is given to the base of $Q_2$. This control voltage adjusts the voltage drop $V_{CE}$ of $Q_2$ till error voltage becomes zero and $V_0$ remains constant.

**iv) Over-Current protection circuit :** Transistor $Q_1$ connected at the output works as current protection circuit. An external resistor $R_{CL}$ connected between its base (current limit) and emitter (current sense) fixes the maximum value of the load current. Under short circuit condition also the load current does not exceed this value.

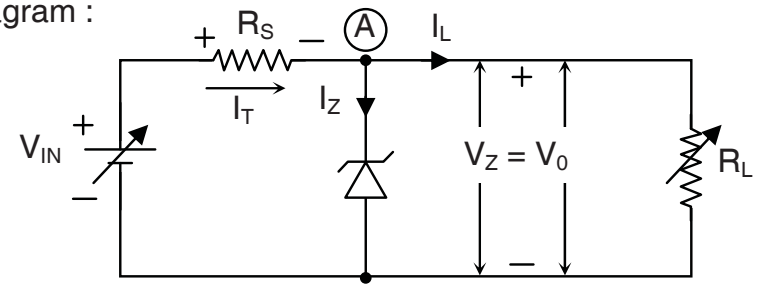
**v) How to vary the output voltage :** A potentiometer $R_2$ is varied to change the output voltage to the required value. This $R_2$ is connected in potential divider circuit across output terminals or it is connected to reference output terminal.

**Q.6 Attempt any FOUR of the following : [16]**

**Q.6(a) Draw the circuit diagram of Zener diode voltage regulator and explain its working. [4]**

**(A) Zener Diode in Parallel to $R_L$**

Circuit Diagram :



**Equations :**

(i) $V_0 = V_Z$ hence if $V_Z$ is constant then $V_0$ is constant.

(ii) By K.C.L. at A , $I_T = I_Z + I_L$

(iii) By K.V.L.,

$\sum$ All voltages = 0

$\therefore \quad V_{IN} - I_T R_S - V_0 = 0$

$\therefore \quad V_0 = V_Z = V_{IN} - I_T R_S \quad$ and $\quad I_T R_S = V_{IN} - V_Z$

$$\therefore \quad R_S = \frac{V_{IN} - V_Z}{I_T} = \frac{V_{IN} - V_Z}{I_Z + I_L}$$

(iv) Thus by selecting the value of $R_S$ properly the condition $I_{Z(knee)} < I_Z < I_{Z(max)}$ is satisfied for all conditions due to which $V_Z = V_0$ remains constant.

**Working :**

**$V_{IN}$ varying $I_L$ constant :** It is assumed that $R_S$ is so selected that $V_0 = V_Z$ = constant.

| | A | B |
|---|---|---|
| 1. | Assume $V_{IN}$ increases. | Assume $V_{IN}$ decreases. |
| 2. | This increases $V_{IN} - V_0$ | This decreases $V_{IN} - V_0$ |
| 3. | $I_T$ increases and $I_T = I_Z + I_L$. But $I_L$ is constant since $V_0$ is constant | $I_T$ decreases and $I_T = I_Z + I_L$. But $I_L$ is constant since $V_0$ is constant. |
| 4. | $I_Z$ increases but $I_Z < I_{Z_{max.}}$ hence $V_0$ is constant | $I_Z$ decreases but $I_Z > I_{Z(knee)}$ hence $V_0$ is constant. |

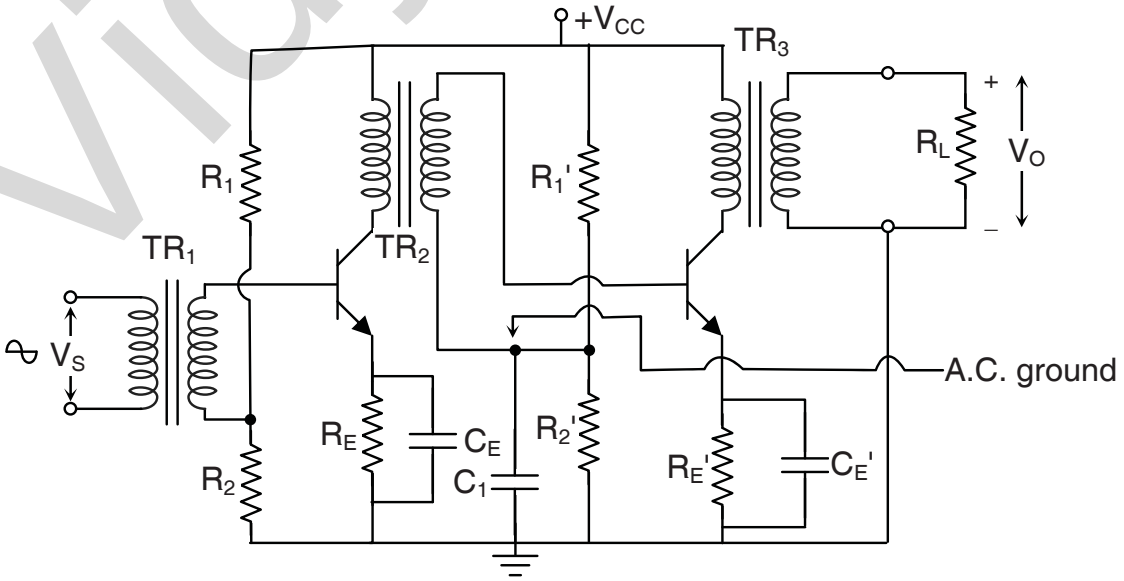
Conditions necessary for this circuit to work properly are

(i) $V_{IN} > V_Z$, so that zener diode is properly reverse biased.

(ii) Value of $R_S$ is so selected that under all conditions; $I_{Z(knee)} < I_Z < I_{Z(max.)}$ is satisfied. Hence zener diode operates in proper breakdown condition and $V_Z = V_0$ remains constant.

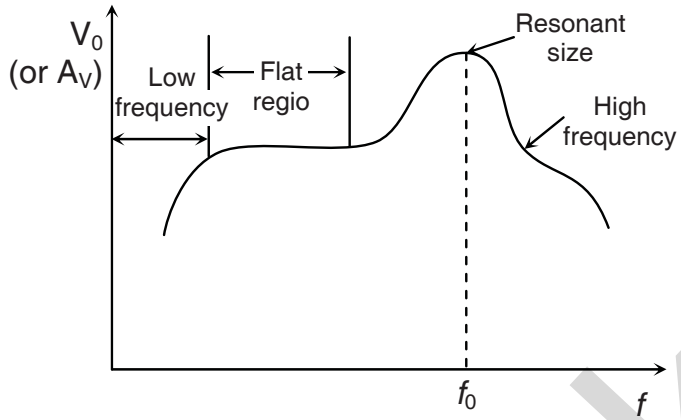
**Q.6(b) Draw the circuit diagram of 2 stage transformer coupled amplifier and explain its working. [4]**

**Q.6(b) 2 stage transformer coupled amplifier**



$TR_1$ : Input transformer
$TR_2$ : Driver transformer
$TR_3$ : Output transformer

**Frequency response**




A transformer is used for coupling the A.C. signal from previous stage to next stage. The main advantages of transformer are :
(i) very good D.C. isolation, (ii) very good impedance matching, (iii) resistance of primary is less hence D.C. losses are less which increases efficiency.
In the above circuit, if $A_{V_1}$ and $A_{V_2}$ are the voltage gains of individual stage then overall voltage gain $A_V = A_{V_1} \times A_{V_2}$. The functions of each component are given below.

(i) $R_1$ and $R_2$ are voltage divider biasing network which establishes Q point in the centre of active region.
(ii) $R_E$ stabilizes Q point.
(iii) $C_E$ by-passes A.C. signal at the emitter. This removes –ve feedback and improves voltage gain.
(iv) Transformer : (a) Gives D.C. isolation, (b) Provides very good impedance matching by selecting number of turns of primary and secondary.
(v) $C_1$ : This capacitor provides A.C. ground due to which maximum A.C. voltage is applied to the $2^{nd}$ stage.

As shown in frequency response, this amplifier is capable of amplifying one particular resonant frequency $f_0$. Hence they are used as tuned voltage amplifiers by connecting capacitors across primary and secondary winding. These are used for amplifying one particular intermediate frequency in communication circuits like Radio, TV, etc.

**Q.6(c) Define voltage gain ($A_V$), current gain ($A_I$) and power gain ($A_P$) of the amplifier and derive the relation between them. [4]**

**(A)** The gain of an amplifier is denoted by "A" and $A = \dfrac{\text{output signal}}{\text{input signal}}$.

(i) Voltage gain $\left( A_V = \dfrac{V_O}{V_{IN}} \right)$ : It is defined as the ratio of output voltage $V_O$ to the input voltage $V_{IN}$. It is a pure number and has no unit of measurement $A_V > 1$ since $V_O > V_{IN}$.

(ii) Current gain $\left(A_I = \frac{I_O}{I_{IN}}\right)$ : It is defined as the ratio of output current $I_O$ to the input current $I_{IN}$. It is a pure number and has no unit of measurement $A_I > 1$ since $I_O > I_{IN}$.

(iii) Power gain $\left(A_P = \frac{P_O}{P_{in}}\right)$ : It is defined as the ratio of output power $P_O$ to the input power $P_{IN}$. It is a pure number and it has no unit of measurement.

**Relation between $A_V$, $A_I$ and $A_P$ –**

Multiplying the values of $A_V$ and $A_I$, we get

$$A_V \times A_I = \frac{V_O}{V_{IN}} \times \frac{I_O}{I_{IN}} = \frac{V_O I_O}{V_{IN} I_{IN}} = \frac{P_O}{P_{IN}} = A_P$$

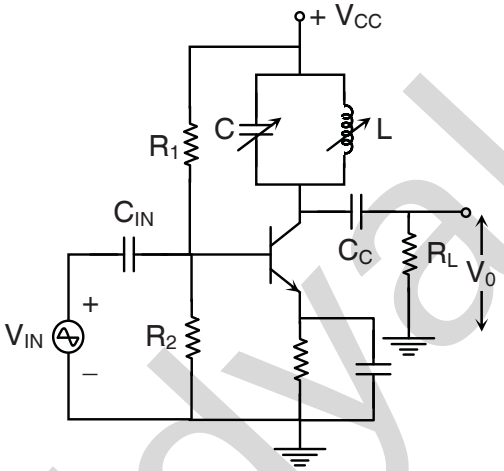
Since $V_O I_O$ = output power $P_O$ and $V_{IN} I_{IN}$ = input power

Thus $A_P = A_V \times A_I$

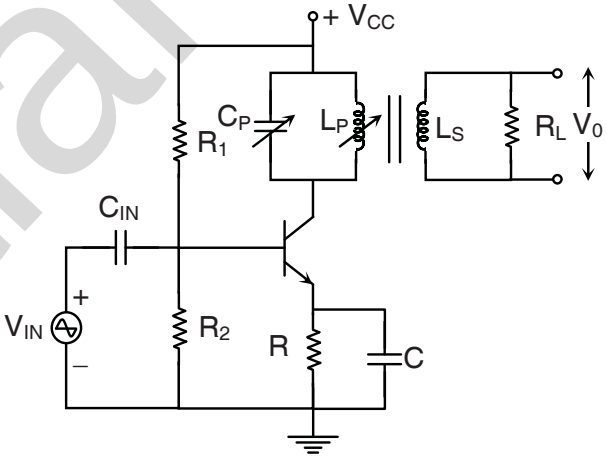
**Q.6(d) Draw the circuit diagram of single tuned voltage amplifier and explain its working with the help of frequency characteristics. [4]**

**(A)** (a) Circuit diagram :

(i) Capacitively coupled



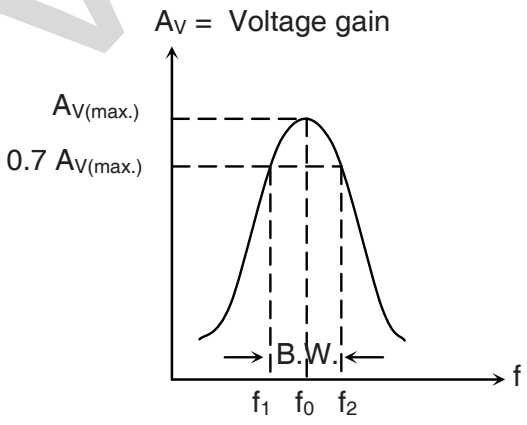

(ii) Inductively coupled




$V_{IN}$ = Modulated high frequency (radio frequency) carrier signal

(b) Frequency Response :

$A_v$ = voltage gain




(i) $f_0$ = Resonant frequency = $f_{IN}$ = carrier frequency

(ii) B.W. = $f_2 - f_1$

(iii) B.W. = $\frac{f_0}{Q_0}$

(iv) $A_v = \frac{\beta_{AC} \times r_L}{R_i}$

(v) $r_L = Z_{eff} = \frac{L}{RC}$ (max.)

**Working :**

Resistors $R_1$ and $R_2$ are voltage divider biasing network which establishes 'Q' point in the centre of active region. $R_E$ stabilizes the 'Q' point. $C_E$ by–passes A.C. signal at the emitter to the ground. This removes –ve feedback due to which $A_v$ increases. $C_{in}$ and $C_c$ block d.c. voltage and allows A.C. voltage to pass.

In the above circuit $R_c$ is replaced by single tuned (parallel resonant) circuit. Either L or C or both are variable. Their values are so adjusted (tuned) that resonant frequency $f_0 = \frac{1}{2\pi\sqrt{LC}}$ of the tuned circuit becomes exactly equal to incoming signal frequency. At $f_0$, $Z_{eff}$ of parallel circuit becomes maximum and is given by $Z_{eff} = \frac{L}{RC}$ where R = resistance of inductor. As shown above $A_v \propto Z_{eff}$ and hence voltage gain becomes maximum at $f_0$ as shown in the frequency response. B.W. = $\frac{f_0}{Q_0}$ and hence as $Q_0$ increases, frequency response becomes more narrower and bandwidth decreases. Hence circuit becomes more selective.

Thus the circuit is capable of amplifying one particular high frequency ($f_0$) or a very narrow band of high frequencies ($f_2 - f_1$). Since only 1 tuned circuit is used. It is known as single–tuned voltage amplifier. The output voltage can be either capacitively coupled or inductively coupled.

**Q.6(e) Give the advantages and dis-advantage of Class B push-pull power amplifier.** **[4]**

**(A) Advantages :**

(i) Maximum power, $\eta$ = 78.4% which is higher than Class A amplifier.
(ii) Even harmonic components are eliminated.
(iii) More A.C. power output per transistor than Class A.
(iv) D.C. current of both transistor flow in opposite direction in the primary winding of output transformer. Hence magnetic fluxes produced by them cancel each other due to which core of transformer does not saturate.
(v) It is possible to eliminate both the transformers which reduces the cost and improves the frequency response.

**Disadvantages :**

(i) Two power transistors are required when increases the cost.
(ii) The two transistors must be a matched pair, i.e., their parameters must be identical to avoid distortion. This also increases the cost of power transistor.
(iii) Driver stage required for producing two equal and opposite A.C. input signals.
(iv) Distortion is more than Class A amplifier.
(v) Because of Class B operation, cross-over distortion present.
(vi) Transformers are bulky and occupy more space.
(vii) Cost increases because of 2 transformers.

**Note :** Since two transformers can be eliminated and A.C. power output is more, Class B push-pull power amplifier are used maximum.

**Q.6(f) Give comparison of class A, B and C power amplifier. [4]**

**(A) Comparison of class A, B and C power amplifier**

| | Parameter | Class A | Class B | Class C |
|---|---|---|---|---|
| 1) | Diagram of A.C. load line. | Refer fig. 1(a). | Refer fig. 1(b). | Refer fig. 1(c). |
| 2) | Q-point | Centre of active region | On the border of cut off and active region | In the cut-off region. |
| 3) | A.C. collector current, $i_C$ | Flows for complete cycle (0 to 360°) | Flows for half cycle (0 to 180°) | Flows for less than half cycle. |
| 4) | D.C. collector current, $I_C$ | Flows even if A.C. input signal is not given. | Does not flow if A.C. input signal absent. | Does not flow if A.C. input signal absent. |
| 5) | Maximum power, $\eta$ | 25% for $R_C$<br>50% for $T_X$<br>(Lowest) | 78.4%<br>(Medium) | > 80%<br>(Highest) |
| 6) | Distortion | Lowest | Medium | Highest |
| 7) | Output power to load. | Lowest | High | Highest |
| 8) | Cross-over distortion | Not present | Present | Not present |
| 9) | Hum (Noise signal) | Absent | Low | High |

❑ ❑ ❑ ❑ ❑