S.Y. Diploma : Sem. III
[DE/ED/EI/EJ/EN/ET/EV/EX/IC/IE/IS/IU/MU]

Principles of Digital Techniques

Prelim Question Paper

Time: 3 Hrs.] **[Marks : 100**

Instructions :
(1) All questions are compulsory.
(2) Illustrate your answers with neat sketches wherever necessary.
(3) Figures to the right indicate full marks.
(4) Assume suitable data if necessary.
(5) Preferably, write the answers in sequential order.

1. (a) Attempt any **SIX** of the following : **[12]**

(i) State the number of Flip Flops required to construct the following modulus of counter :
(1) 7 (2) 85 (3) 98 (4) 11

(ii) Draw symbol and truth table of :
(1) AND gate (2) NOR gate

(iii) State the different triggering methods in digital circuit.

(iv) Define the following terms : (1) Propagation delay
(2) Fan-out

(v) Define : (1) Minterm (2) Maxterm

(vi) Convert given SOP equation in standard SOP equation :
$Y = \overline{A}BC + B\overline{C} + AC$

(vii) Write associative and commutative Boolean laws.

(viii) State any two features of PCF 8591.

(b) Attempt any **TWO** of the following : **[8]**

(i) Explain Full adder with its truth table, K–map simplification and logic diagram.

(ii) Design a 3 : 8 decoder using Basic Logic Gates ?

(iii) Design a 4 : 1 MUX using 2 : 1 MUX and write truth table.

2. Attempt any **FOUR** of the following : **[16]**

(a) Prove that : $ABC + ABD + \overline{A}B\overline{C} + CD + B\overline{D} = B + CD$

(b) Implement function of OR using NAND.

(c) Design Delay Flip Flop, using RS Flip-flop.

(d) Define triggering methods.

(e) State and prove the both De-Morgan's theorems with logic diagram.

(f) Define the following specifications of DAC :
(i) Resolution (ii) Linearity
(iii) Accuracy (iv) Setting time

3. Attempt any **FOUR** of the following : **[16]**

(a) Differentiate between Combinational Circuits and Sequential Circuits.

(b) Perform following BCD operations:

(i) $\begin{array}{r} 16 \\ +\ 27 \end{array}$ (ii) $\begin{array}{r} 35 \\ +\ 19 \end{array}$

(c) Design 1 : 16 demultiplexer using 1 : 4 demultiplexer.

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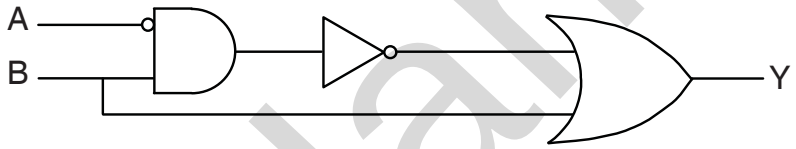
(d) Simplify given SOP equation using K-map technique-
$Y = \Sigma m\ (0, 1, 2, 3, 4, 5, 7, 12, 13, 15)$
(e) State advantages and disadvantages of single slope ADC.
(f) Describe the working of 4-bit ripple counter with logic diagram and waveforms.

4. Attempt any **FOUR** of the following : **[16]**
(a) Subtraction using 1's and 2's complement method :
(i) $(52)_{10} - (65)_{10}$ (ii) $(101011)_2 - (11010)_2$
(b) Implement 1:32 DeMux using 1:8 DeMux only.
(c) What is race around condition in JKFF? How it can be avoided?
(d) State the rules for BCD addition.
(e) Describe successive approximation ADC with neat circuit diagram.
(f) Draw the logic diagram of 4-bit SIPO shift register and explain its working principle.

5. Attempt any **FOUR** of the following : **[16]**
(a) Draw and explain the circuit diagram of 1 : 4 demultiplexer using logic gates.
(b) (i) Write the sop expression for the below circuit diagram.



(ii) Which is the fastest logic family out of all logic families and why?
(c) Draw the diagram of 3 bit ripple counter and write its operation.
(d) Draw the circuit of master slave JK FF using NAND gate and list its advantages.
(e) Implement the following function using demultiplexer.
$F_1 = \sum m\ (1, 2, 5, 6, 7, 11, 14)$
$F_2 = \pi\ M\ (0, 1, 2, 5, 6, 7, 8, 11, 12, 15)$
(f) Compare volatile and non-volatile memory (any 4 points).

6. Attempt any **FOUR** of the following : **[16]**
(a) Convert the following :
(i) $(5C7)_{16} = (?)_{10}$ (ii) $(2598)_{10} = (?)_{16}$
(iii) $(10110)_2 = (?)_{10} = (?)_{16}$
(b) Describe the working of BCD to 7 segment decoder with truth table and circuit diagram.
(c) Reduce the following Boolean expression using Boolean laws :
(i) $Y = A\bar{B} + \bar{A}B + AB + \overline{AB}$ (ii) $Y = A\bar{B}C + \bar{A}BC + ABC$
(d) Explain the method of operation of a Single Slope ADC?
(e) Describe working of 4-bit asynchronous Up-Down counter.
(f) Draw the circuit diagram of 4-bit R-2R ladder DAC and obtain its output voltage expression.

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