S.Y. Diploma : Sem. III

[CO/CM/CW/DE/EJ/ET/EN/EX/EQ/IE/IS/IC/MU]

# Digital Techniques

**Time: 3 Hrs.]** Prelim Question Paper - Solution **[Marks : 70**

**Q.1 Attempt any FIVE of the following : [10]**

**Q.1(a) Write the 1's complement and 2's complement of $(10111)_2$ [2]**

**Ans.:**

1 0 1 1 1 1

↓ Replacing 1 by 0 & 0 by 1

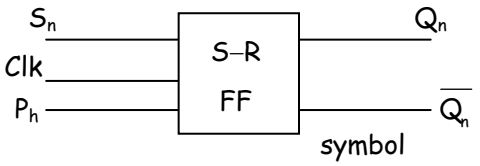
0 1 0 0 0 0 ⟶ 1's complement

\+ 1 ⟶ Adding 1

0 1 0 0 0 1 ⟶ 2's complement

**Q.1(b) Draw symbol and write the truth table of S-R flip-flop. [2]**

**Ans.:**




symbol

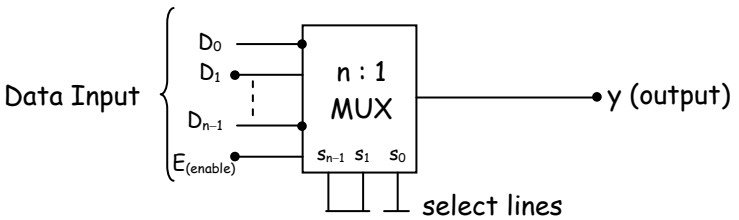
Truth table of S-R FF

| Clk | $S_n$ | $R_n$ | $Q_{nH}$ |
|---|---|---|---|
| 0 | X | X | $Q_n$ |
| 1 | 0 | 0 | $Q_n$ (No charge) |
| 1 | 0 | 1 | 0 (Reset) |
| 1 | 1 | 0 | 1 (set) |
| 1 | 1 | 1 | (Forbidden) |

**Q.1(c) Explain why multiplexers are needed in digital electronic system. [2]**

**Ans.:** Need of MUX

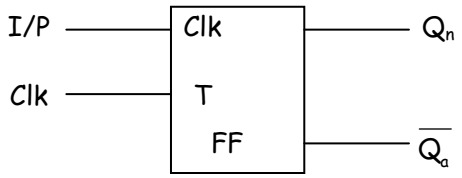
- The multiplexer (or data selector) is a logic circuit that transfer several input to a single O/P.



- MUX are used in communication to allow channel sharing.
- MUX are used in parallel to serial data convertors.
- MUX are also used in waveform generators.

**Q.1(d) Write excitation table for T flip-flop.** **[2]**

**Ans.:**




Symbol of TFF

**Excitation Table**

| $Q_n$ | $Q_{n+1}$ | T |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

**Q.1(e) With reference to ADC, define accuracy and conversion time.** **[2]**

**Ans.:** Accuracy : It is a comparison of actual output voltage with expected output.

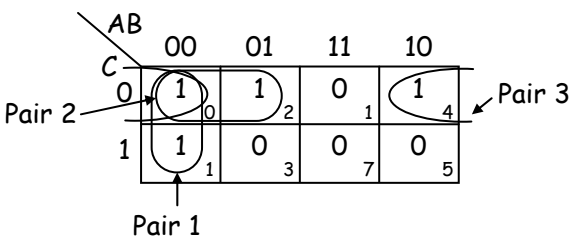
$$\text{Accuracy} = \frac{V_{ofs}}{(2^n - 1)^2}$$

Conversion Time : It is a time required for conversion of analog signal into its digital equivalent. It is also called as setting time.

**Q.1(f) Simply using k-map** **[2]**

**f(A, B, C) = ∑m(0, 1, 2, 4)**

**Ans.: 3–Variable K-map**




$\therefore$ $f(A, B, C) = \bar{A}\bar{B} + \bar{A}\bar{C} + \bar{B}\bar{C}$

**Q.1(g) Define modulus of a counter 1, Write down the number of flip-flop required for M-10 counter 7.** **[2]**

**Ans.: Modulus (MOD) of counter :**

Modulus of a counter represents the number of states through which the counter progresses during its operation.

For MOD – N Counter

$N \leq 2^m$

m $\rightarrow$ No. of flip–flops required

$\therefore$ $10 \leq 2^m$

$\therefore$ m = u

$\therefore$ For MOD–10 counter 4 flip flop are required.

**Q.2 Attempt any Three of the following :** **[12]**

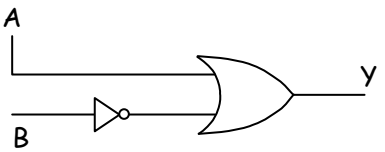
**Q.2(a) Simplify using Boolean laws and draw logical diagram** **[4]**

**$ABC + ABC + \bar{A}\bar{B}\bar{C} + A\bar{B}C + A\bar{B}\bar{C} + \bar{A}\bar{B}C + AB\bar{C}$**

**Ans.:** Let

$$\begin{aligned} Y &= ABC + ABC + \bar{A}\bar{B}\bar{C} + A\bar{B}C + A\bar{B}\bar{C} + \bar{A}\bar{B}C + AB\bar{C} \\ &= ABC + \bar{A}\bar{B}\bar{C} + A\bar{B}C + A\bar{B}\bar{C} + \bar{A}\bar{B}C + AB\bar{C} \\ &= AB(C + \bar{C}) + \bar{A}\bar{B}(\bar{C} + C) + A\bar{B}(C + \bar{C}) \\ &= AB \cdot 1 + \bar{A}\bar{B} \cdot 1 + AB \cdot 1 \\ &= AB + \bar{A}\bar{B} + A\bar{B} \\ &= AB + \bar{B}(\bar{A} + A) \\ &= AB + \bar{B} \cdot 1 \\ &= \bar{B} + AB \\ Y &= A + \bar{B} \end{aligned}$$

Logical Diagram



**Q.2(b) Design 4-bit binary number to 4-bit gray number.** **[4]**

**Ans.: Truth Table**

| Decimal | Binary | | | | Gray | | | |
|---|---|---|---|---|---|---|---|---|
| | $B_3$ | $B_2$ | $B_1$ | $B_0$ | $G_3$ | $G_2$ | $G_1$ | $G_0$ |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 |
| 2 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1 |
| 3 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 |
| 4 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 0 |
| 5 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 1 |
| 6 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 1 |
| 7 | 0 | 1 | 1 | 1 | 0 | 1 | 0 | 0 |
| 8 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 |
| 9 | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 1 |
| 10 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | 1 |
| 11 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 0 |
| 12 | 1 | 1 | 0 | 0 | 1 | 0 | 1 | 0 |
| 13 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 1 |
| 14 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 1 |
| 15 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 |

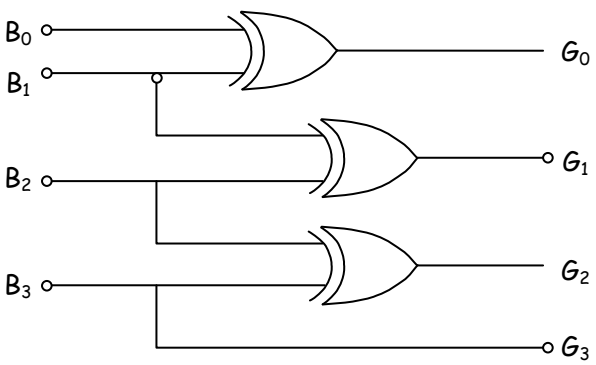
From k-map

$G_3 = B_3$

$G_2 = B_3 \oplus B_2$

$G_1 = B_2 \oplus B_1$

$G_0 = B_1 \oplus B_0$

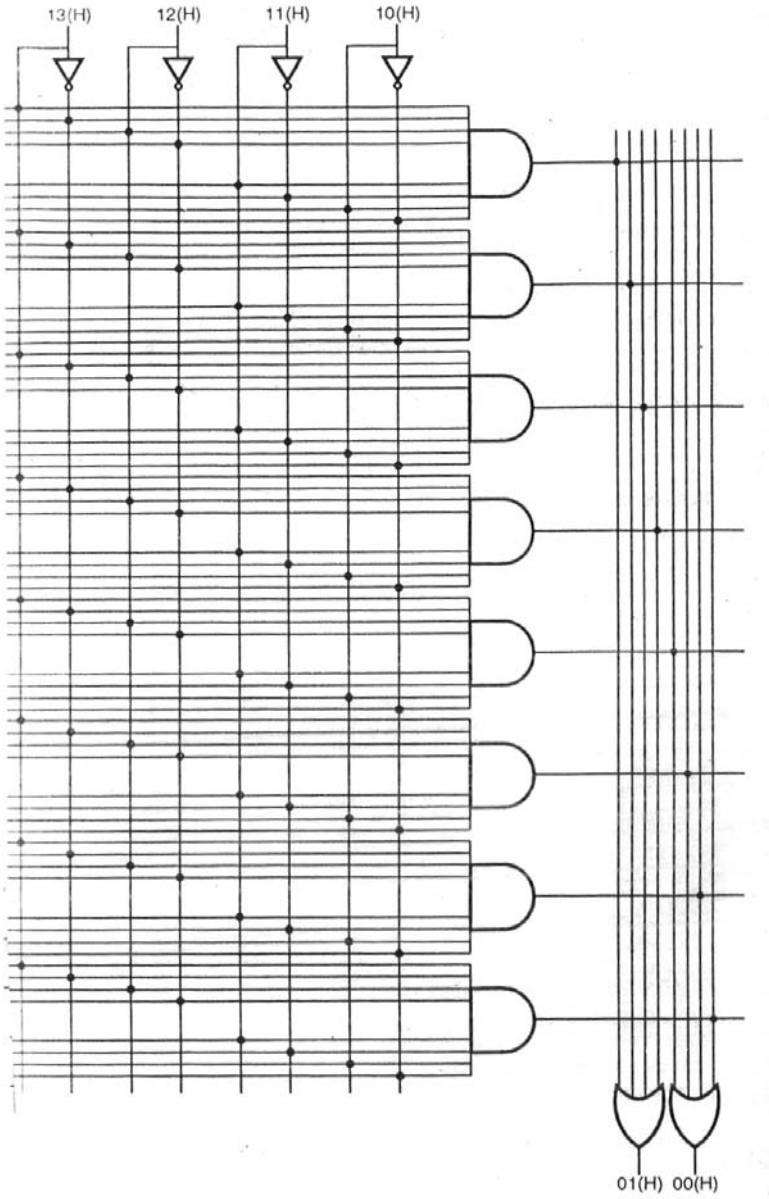



Logic Circuit

**Q.2(c) Draw and explain PAL.** **[4]**

**Ans.:** The PAL represents another alternative to PROMs. This device was introduced by monolithic memories.

The PAL suffers from the PROM in that the input AND gate connections are programmable in PAL, Whereas the output OR gate connectors are programmable in PROM.

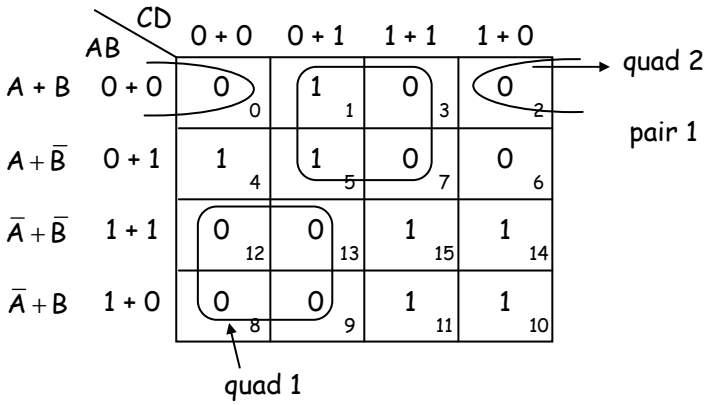



**Example of PAL**

**Q.2(d) Minimize the following expression using k-map** **[4]**

**f(A, B, C, D) = πM(0, 2, 3, 6, 7, 8, 9, 12, 13)**

**Ans.:**

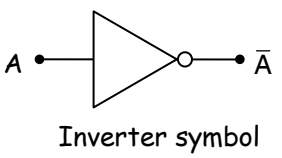



$\therefore \quad f(A, B, C, D) = (\bar{A} + C)(A + \bar{C})(A + B + D)$

**Q.3 Attempt any Three of the following :** **[12]**

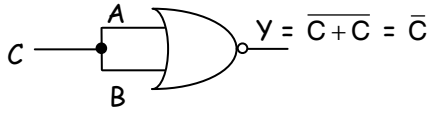
**Q.3(a) Realize the following logic operations using only NOR gates : AND, OR, NOT.** **[4]**

**Ans.: (i) NOT Gate**



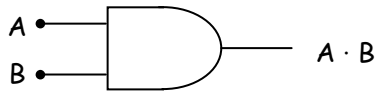

Input Output

| A | Ā |
|---|---|
| 0 | 1 |
| 1 | 0 |

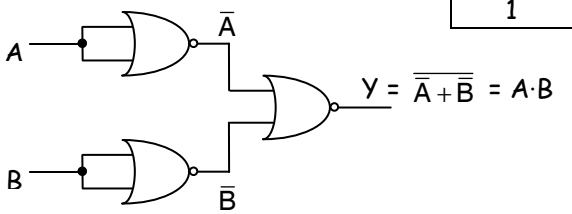



Input

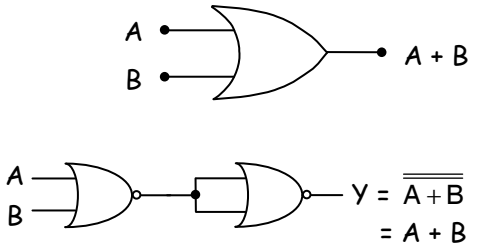
**(ii) AND Gate**




| A | B | A · B |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 1 |



**(iii) OR Gate**




| A | B | A + B |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 1 |

**Q.3(b) Compare TTL and CMOS logic families on the basis of following [4]**

**(i) Propagation delay**

**(ii) Power dissipation (per gate)**

**(iii) Fan out**

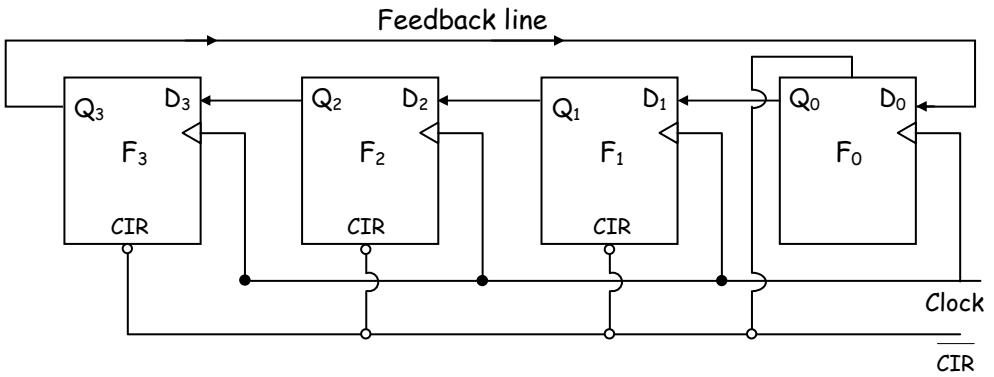
**(iv) Basic Gate**

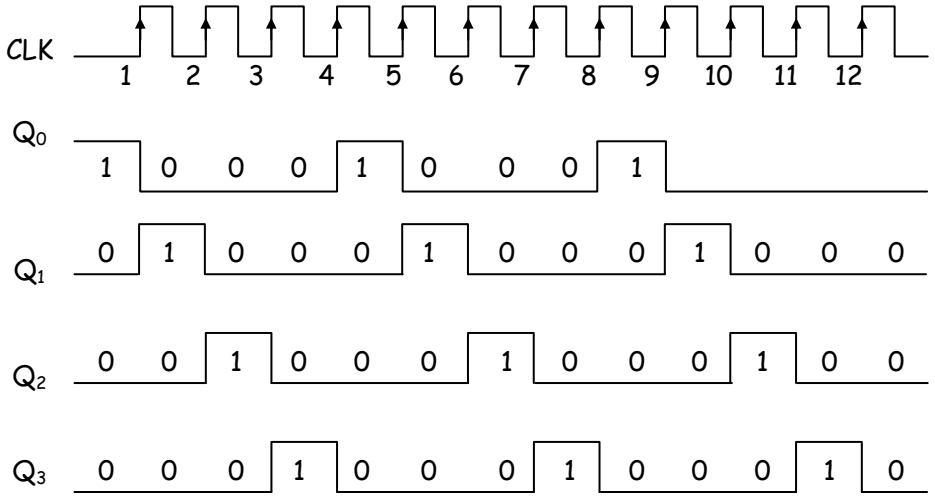
**Ans.:**

| | Parameter | TTL | CMOS |
|---|---|---|---|
| (i) | Propagation delay | 10 n sec | 105 n sec |
| (ii) | Power dissipation (per gate) | 0.1 mW | 10 mW |
| (iii) | Fan out | More than 50 | 10 |
| (iv) | Basic Gate | NAND/NOR | NAND |

**Q.3(c) Draw the circuit diagram and draw waveform for ring counter. [4]**

**Ans.:**






Basically ring counter resembles shift register because the bits are shifted left one position per positive clock edge. Only change is feedback line i.e. output of $Q_3$ given to $Q_0$.

**Q.3(d) Calculator analog output of 4 bit DAC for digital input 1010. Assume $V_{FS}$ = 5V. [4]**

**Ans.: Given Digital Data**

1 0 1 0

$d_1$ $d_2$ $d_3$ $d_4$

For 4–bit DAC the output voltage

$$V_0 = V_{FS}\left[d_1 2^{-1} + d_2 2^{-2} + d_3 2^{-3} + d_4 2^{-4}\right]$$

$$v_0 = 5\left[1\times 2^{-1} + 0\times 2^{-2} + 1\times 2^{-3} + 0\times 2^{-4}\right] = 5\left[\frac{1}{2} + 0 + \frac{1}{2^3} + 0\right] = 5\left[\frac{1}{2} + \frac{1}{8}\right]$$

$V_0$ = 3.125 V

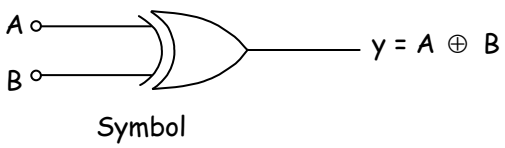
**Q.4 Attempt any Three of the following : [12]**

**Q.4(a) Draw the symbol and write logic expression and truth table of the two input Ex-OR and Ex-NOR Gates. [4]**

**Ans.: Exclusive OR Gate (Ex–OR)**

Truth Table

| A | B | y = A ⊕ B |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |




Symbol

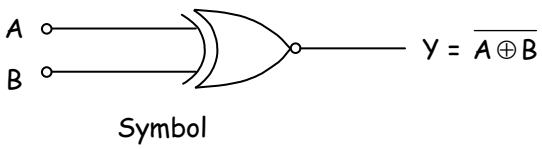
Output expression, $Y = A \oplus B$

$Y = A\bar{B} + \bar{A}B$

Exclusive NOR Gate (Ex–NOR)

Truth Table

| A | B | $Y = \overline{A \oplus B}$ |
|---|---|---|
| 0 | 0 | 1 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 1 |



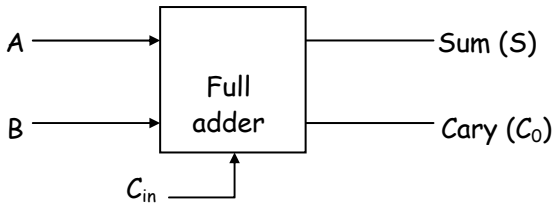

Symbol

Output expression, $Y = \overline{A \oplus B}$

$Y = AB + \bar{A}\bar{B}$

**Q.4(b) Describe function of full adder with its truth table, k-map simplification and logic diagram. [4]**

**Ans.:**




The full adder is a three input and two output combination circuit

**Truth Table**

| **Inputs** | | | **Output** | |
|---|---|---|---|---|
| A | B | $C_{in}$ | S | $C_o$ |
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 | 0 |
| 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 | 1 |
| 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 0 | 1 |
| 1 | 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 1 | 1 |

**K-map or sum output**

| A \ $BC_{in}$ | 00 | 01 | 11 | 10 |
|---|---|---|---|---|
| 0 | 0 (0) | 1 (1) | 0 (3) | 1 (2) |
| 1 | 1 (4) | 0 (5) | 1 (7) | 0 (6) |

$$S = \bar{A}\bar{B}C_{in} + \bar{A}B\bar{C}_{in} + ABC_{in} + A\bar{B}\bar{C}_{in} = C_{in}(\bar{A}\bar{B} + AB) + \bar{C}_{in}(\bar{A}B + A\bar{B})$$

$$S = C_{in}(A \odot B) + \overline{C_{in}}(A \oplus B) \qquad = C_{in}\left(\overline{A \oplus B}\right) + \overline{C_{in}}(A \oplus B)$$

$$S = A \oplus B \oplus C_{in}$$

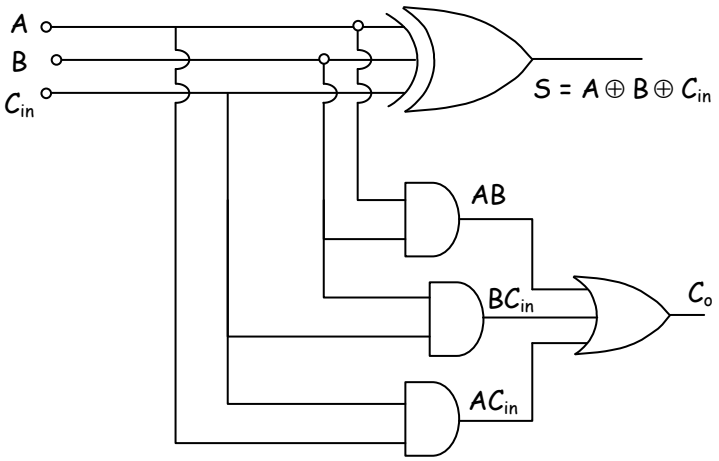
k–map for carry ($C_0$)

| A \ $BC_{in}$ | 00 | 01 | 11 | 10 |
|---|---|---|---|---|
| 0 | 0 (0) | 0 (1) | 1 (3) | 0 (2) |
| 1 | 0 (4) | 1 (5) | 1 (7) | 1 (6) |

$AC_{in}$ AB

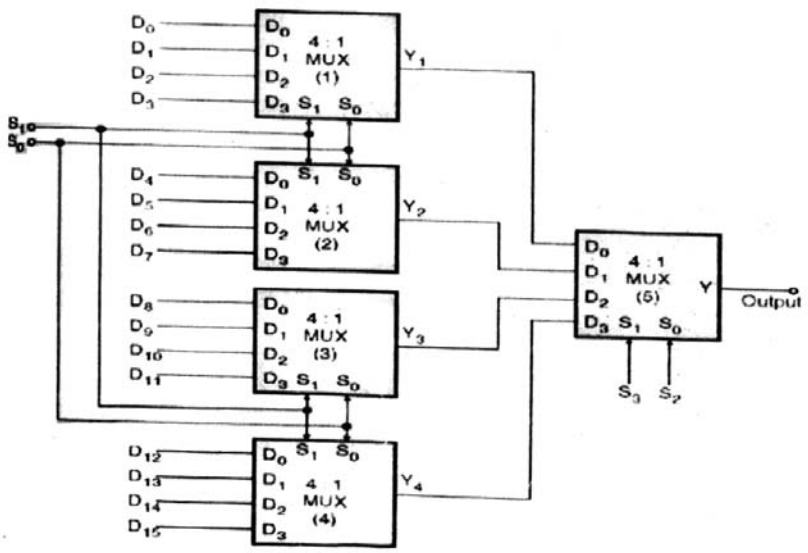
$C_0 = AB + AC_{in} + BC_{in}$

Logic diagram for full adder



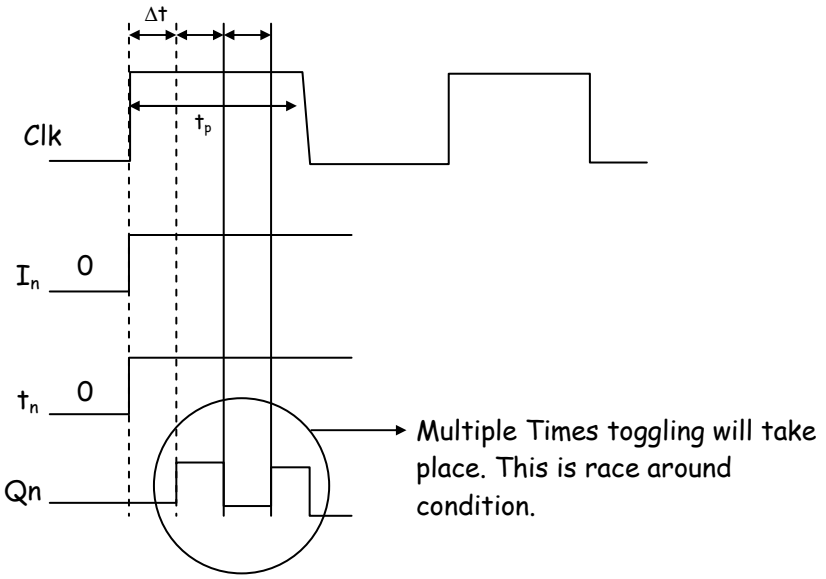
**Q.4(c) Design 16:1 mux using 4:1 mux.** **[4]**

**Ans.:**




**Q.4(d) With reference to JK flip flop, explain race–around condition** **[4]**

**Ans.:** Consider JK FF with $J_n$ = $K_n$ = 1 and $Q_n$ = 0 and pulses as shown below is applied at the clock input.



- After a time interval $\Delta t$ equal to the propagation delay through two AND gates in series, the output will change to Q = 1
  Now we have $J_n = k_n = 1$ and Q = 1 and after another time interval o $\Delta t$ the output will change back to Q = 0
  Hence we conclude that for the duration $t_p$ of the clock pulse the output will oscillate back and forth between 0 and 1,
- At the end of the clock pulse, the value of Q is uncertain, This situation is referred to as the race–around condition.
- Race – around condition can be overcomed by using master–slave (M-S) J-K FF

**Q.4(e) What are the advantages of successive approximation ADC? An 8 bit successive approximation ADC is driven by a MHz. Find its conversion time.** **[4]**

**Ans.: Advantages of successive approximate ADC**

(1) Speed of conversion is fast
(2) Resolution is upto $2^{16}$
(3) It user very efficient code searching strategy called binary search. It completes searching process or n-bit conversion m just n clock periods.

Given :

$f = 1\ MH_2$

$T = \frac{1}{f} = \frac{1}{1\times10^6} = 1\ \mu sec$

$n = 8$

$T_c = T(n + 1) = 1\ \mu se(8 + 1)$

$T = 9\ \mu sec$

**Q.5 Attempt any TWO of the following :** **[12]**

**Q.5(a) Design mod-3 Asynchronous counter and draw output waveform.** **[6]**

**Ans.:** Design mod –3 Asynchronous counter and draw output waveform.
To design mod-3 counter we required 2 flip-flops

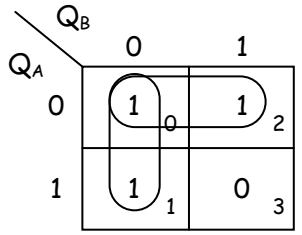
| $Q_B$ | $Q_A$ | | | |
|---|---|---|---|---|
| 0 | 0 | → 0 | → | Valid |
| 0 | 0 | → 1 | → | Valid |
| 0 | 0 | → 2 | → | Valid |
| 1 | 1 | → 3 | → | Invalid state |

∴ Design a reset logic combinational circuit such that output y should be 1 when valid states are there and y = 0 when invalid states are present.

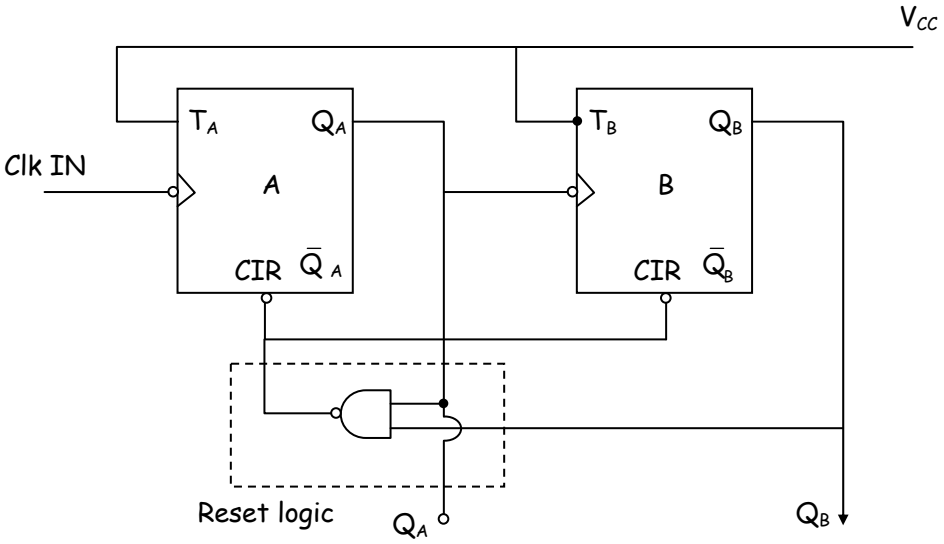
Truth table

| $Q_B$ | $Q_A$ | y(output) |
|---|---|---|
| 0 | 0 | 1 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

K-map




$y = \overline{A} + \overline{B} = \overline{AB}$




**Q.5(b) (i) Compare volatile and Non-Volatile memory. [6]**

**(ii) Compare EPROM and EEPROM.**

**Ans.: (i) Compare volatile and Non-Volatile memory.**

| | Parameter | Volatile | Non-Volatile |
|---|---|---|---|
| 1. | Definition | Information is if power is turned off. | Information is not lost if power is turned off. |
| 2. | Classification | All RAMS | ROMs, EPROM, magnetic memories. |
| 3. | Effect of power | Stored information is retained only as long as power is on. | No effect of power on stored information. |
| 4. | Applications | For temporary storage. | For permanent storage of information. |

**(ii) Compare EPROM and EEPROM.**

| Parameters | EPROM | EEPROM |
|---|---|---|
| Technique used for erasing | Exposure to ultraviolet light. | A voltage of 20 to 25 V is applied. |
| Selective erasing | Not possible. All the locations get erased. | Possible. A particular location only can be erased. |

**Q.5(c) Perform the following operation :** **[6]**

**(i) $(11100)_2 \div (100)_2$**

**(ii) $(1010.11)_2 \times (11)_2$**

**(iii) $(1011.11)_2 + (1100.01)_2$**

**Ans.: (i) $(11100)_2$ / $(100)_2$**

```
        1 1 1
    ___________
100 ) 1 1 1 0 0
      - 1 0 0
      ---------
        0 1 1 0
      - 1 0 0
      ---------
          0 1 0 0
        - 1 0 0
        ---------
            0 0 0
```

Therefore, Quotient = $(111)_2 = (7)_{10}$

Remainder = $(000)_2 = (0)_{10}$

**(ii) $(1010.11)_2 \times (11)_2$**

```
      1 0 1 0.1 1
  ×         1 1
  ---------------
    1 0 1 0 1 1
  1 0 1 0 1 1 -
  -------------
      1 1 1 1 1
  -------------
  1 0 0 0 0 0.0 1
```

Therefore, $(1010.11)_2 \times (11)_2 = (100000.01)$

**(iii) $(1011.11)_2 + (1100.01)_2$**

```
      1 0 1 1 . 1 1
+     1 1 0 0 . 0 1
    [1][1][1][1] [1]
-----------------------
  1 1 0 0 0 . 0 0   ⟶ result
```

**Q.6 Attempt any TWO of the following : [12]**

**Q.6(a) How can JC 7490 can used as a decade counter with neat block diagram. [6]**

**Ans.: Explanation**

**IC 7490 :** It consists of two counters namely MOD 2 and MOD 5. Thus IC 7490 can be used as MOD 2 or MOD 5 counter independently. Ehen this IC need to be used as MOD 10 i.e. decade counter, the o/p of MOD 2 counter i.e. $Q_A$ need to be connected to the clock i/p of MOD 5 counter as shown below thus acting as a 4 bit MOD 10 counter.

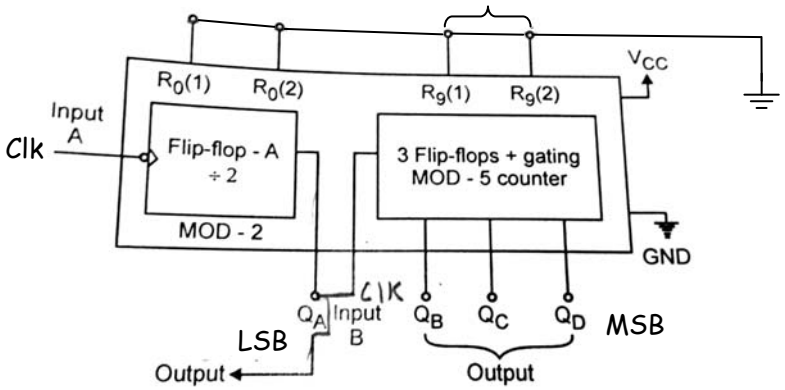



**Fig.:** IC 7490 be used as a decade counter

Truth table

| Decimal input | BCD/decimal output | | | |
|---|---|---|---|---|
| | D | C | B | A |
| 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 0 | 1 |
| 2 | 0 | 0 | 1 | 0 |
| 3 | 0 | 0 | 1 | 1 |
| 4 | 0 | 1 | 0 | 0 |
| 5 | 0 | 1 | 0 | 1 |
| 6 | 0 | 1 | 1 | 0 |
| 7 | 0 | 1 | 1 | 1 |
| 8 | 1 | 0 | 0 | 0 |
| 9 | 1 | 0 | 0 | 1 |
| 0 | 0 | 0 | 0 | 0 |

**Q.6(b) Draw the block diagram of dual slope ADC and explain its working with waveforms. [6]**

**Ans.:** The dual slope ADC consists of OPAMP is being used as integrator and comparator. The control logic accepts the SOC signal and generates EOC

signal when the conversion is over. It also controls the two switches S1 and S2 out of which S1 is a single pole three way switch whose one terminal is connected to analog voltage VA, second one is connected to ground and the third one is connected to a negative reference voltage VREF

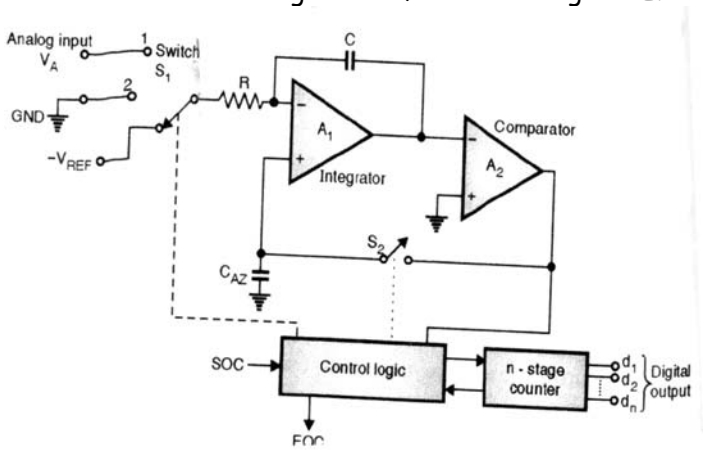
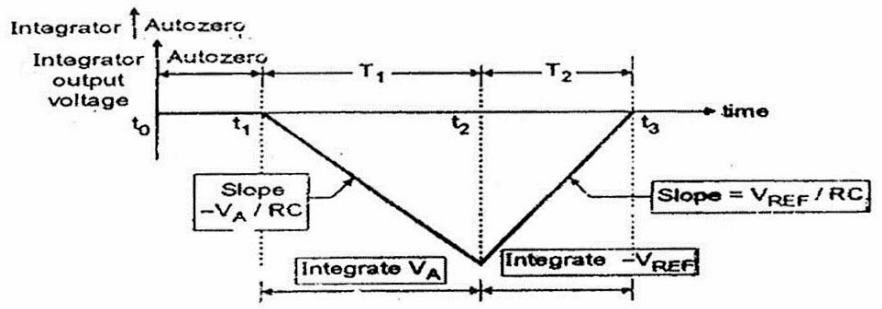



**Fig.:** Dual Slope ADC

**Operation:**

At the out Initially assume that the integrator output voltage $V_0$= 0 and the counter is in RESET condition i.e. counter output is 00.

1. At t = t0 switch S1 is connected to ground and switch $S_2$ is closed. The capacitor CAZ gets connected across the comparator output.
2. Any offset voltage present in the OP-AMPs will appear across the capacitor C. This will provide an automatic compensation for the input offset voltage of all the amplifiers. Therefore integrator output voltage is zero for the interval $t_0$ to $t_1$.
3. At instant t1 the SOC command is given to the control logic. Switch S1 is connected to $V_A$ and Switch $S_2$ is open circuited. CAZ acts as a memory to hold the voltage required to keep the offset zero. Hence CAZ is known as the auto zero capacitor.
4. From $t_1$ to $t_2$, this ADC will integrate the analog input $V_A$, for a fixed duration of clock cycles. This time interval is requited for the counter to advance through all its possible output states, because for an n-bit counter there will be 2n possible output states.
5. The counter output then reduces to zero. The time duration $t_1$ to $t_2$ t is represented by $T_1$.The integrator output during this period is given by,




$$V_O = -\frac{1}{RC}\int_{t_1}^{t_2} V_A \, dt = \frac{-V_A T_1}{RC}$$

This expression represents a straight line with a slope of - $V_A$ / $R_C$. Thus we get a decreasing ramp. The time period T is thus represented by 2n clock cycles.

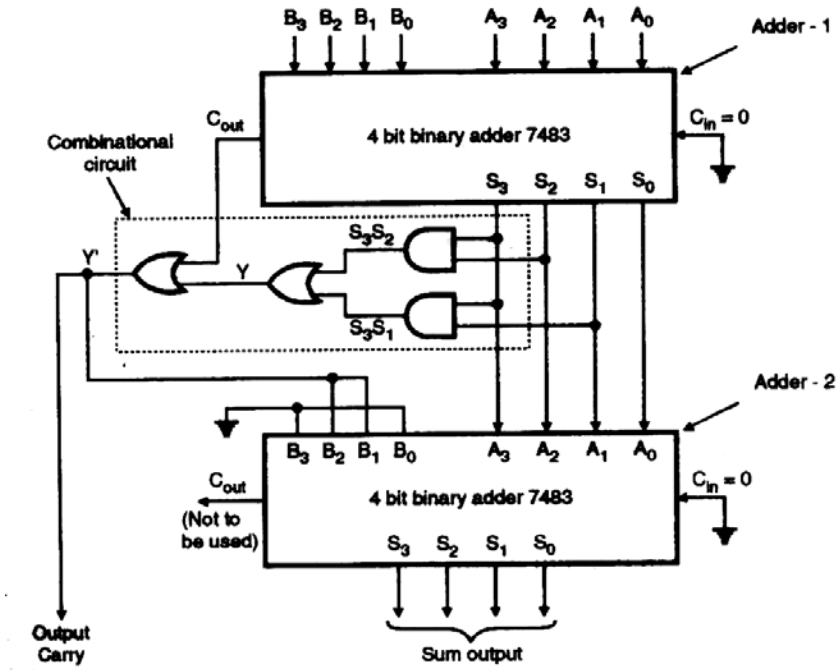
$\therefore \quad T_1 = 2^n \times T$ … Where T = one clock cycle period

6. At the end of interval $T_1$ the integrator input is connected to a fixed negative reference voltage ($-V_{REF}$) via switch $S_1$.
7. The integrator output now starts increasing towards zero with positive slope. The slope of the line is $V_{REF}$ / $R_C$ for the duration $t_2$ to $t_3$.
8. The counter starts counting from 0. The integration will continue till the integrator output is non-zero. At instant $t_3$ the integrator output reduces to zero then the comparator output goes from HIGH to LOW and the clock pulses given to the counter are stopped.
9. At $t_3$ the counter output shows a number corresponding to N clock cycles it has counted during period $t_2$ to $t_3$.
10. Thus this number N represents the time taken for integrator output to reduce from $-V_A$ to 0. Hence N represents the desired digital output code proportional to the analog input $V_A$.
12. If $V_A$ increases, then the integrator capacitor vi1l charge to a higher negative voltage during the time interval T Therefore the time T required to reduce the integrator output to zero increases.
13. Therefore the counter output count (N) will be higher. Thus N is proportional to $V_A$.

**Q.6(c) Describe the operation of single digit BCD adder using IC – 7483 [6] with circuit diagram.**

**Ans.: Single digit BCD adder using IC – 7483**

**Circuit diagram :**




**Operation :**

- A BCD adder adds two BCD digits and produces a BCD digit.
- The two given BCD numbers are to be added using the rules of binary addition.
- If sum is less than or equal to 9 and carry=0 then no correction is necessary.The sum is correct and in the true BCD form.
- But if sum is invalid BCD or carry=1 then the result is wrong and needs correction.
- The wrong result can be corrected by adding six(0110) to it.

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