T.Y. Diploma : Sem. VI [EJ/ET/EX/EN/EI/IE]

Very Large Scale Integration

Time : 3 Hrs. Prelim Question Paper **Marks : 100**

Instructions :(1) All questions are compulsory.
(2) Answer each next main question on a new page.
(3) Illustrate your answers with neat sketches wherever necessary.
(4) Figures to the right indicate full marks.
(5) Assume suitable data, if necessary.
(6) Mobile Phone, Pager and any other Electronic Communication devices are not permissible in Examination Hall.

1. (a) Attempt any **THREE** questions. **[12]**
(i) Differentiate between Xiliv and Atmel series architecture of CPLD. (four points)
(ii) Compare synchronous and asynchronous sequential circuit on the basis of :
(i) Definition (ii) Clock requirement
(iii) Output affected by (iv) Memory element
(iii) What is Test bench and write down a typical test bench format.
(iv) Write VHDL code to implement 4:1 multiplexer.
(v) List and explain data types used in HDL.

1. (b) Attempt any **ONE** questions. **[6]**
(i) Design a sequence detector to detect the sequence 101.
(ii) Draw architecture of CPLD and explain in brief.

2. Attempt any **FOUR** questions. **[16]**
(a) Write VHDL code for 3-bit up-counter.
(b) Explain P well process with suitable diagram.
(c) What is event scheduling and zero modelling.
(d) List the features of FPGA.
(e) (i) Give the syntax of signal used in VHDL.
(ii) Write the syntax of CASE statement.
(f) Explain the shift operations and logical operations.

3. Attempt any **FOUR** questions. **[16]**
(a) Explain HDL design flow for synthesis.
(b) Draw CMOS AND Gate and write it with Truth Table. (2 input)
(c) Design $Z = \overline{XY + UV}$ using CMOS logic.
(d) Draw 3 : 8 decoder and write VHDL code for it.
(e) Define the following terms :
(i) Meta stability (ii) Set-up time (iii) Hold time (iv) Fan-out
(f) Explain various operators used in VHDL.

4. (a) Attempt any **THREE** questions. **[12]**
(i) Explain Twin-tube process with suitable diagram.
(ii) Explain Event based and cycle based simulator.
(iii) Explain sensitivity list and zero modeling.
(iv) Draw full Adder using gates and write VHDL code for it.

(b) Attempt any **ONE** questions. **[6]**
(i) Explain CZ process for wafer fabrication, with neat diagram.
(ii) List and explain the main steps carried in typical n-well, CMOS fabrication process with neat sketches.

5. Attempt any **FOUR** questions. **[16]**

(a) Define following terms related to fabrication process.
  (i) Oxidation (ii) Diffusion
  (iii) Ion-implantation (iv) Deposition

(b) Define the following terms.
  (1) Metastability (2) Noise Margin

(c) Compare BJT and CMOS.

(d) Write VHDL program to Implement JK flip-flop with + ve edge trigger.

(e) Explain the basic architecture of SPARTAN – 3 FPGA series.

(f) Compare FPGA and CPLD.

6. Attempt any **FOUR** questions. **[16]**

(a) Explain with syntax.
  (1) Entity (2) Architecture

(b) Compare Mealy Machine with Moore Machine.

(c) Draw and explain working of CMOS Transmission gates.

(d) Draw and Implement the T flip-flop using Moore machine.

(e) Draw the general FPGA chip architecture and explain the same.

(f) Compare software and hardware description languages.

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