Q.1(a) Explain why multiplexers are needed in digital electronic system. [2]
Ans.: Need of MUX
- The multiplexer (or data selector) is a logic circuit that transfers several inputs to a single O/P.
- MUX are used in communication to allow channel sharing.
- MUX are used in parallel to serial data converters.
- MUX are also used in waveform generators.

Q.1(b) With reference to ADC, define accuracy and conversion time. [2]
Ans.: Accuracy : It is a comparison of actual output voltage with expected output.

\[
\text{Accuracy} = \frac{V_{ofs}}{(2^n - 1)^2}
\]

Conversion Time : It is a time required for conversion of analog signal into its digital equivalent. It is also called as setting time.

Q.1(c) List the binary, octal and hexadecimal numbers for decimal no. 0 to 15. [2]
Ans.:

<table>
<thead>
<tr>
<th>DECIMAL</th>
<th>BINARY</th>
<th>OCTAL</th>
<th>HEXADECIMAL</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0000</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>0001</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>2</td>
<td>0010</td>
<td>2</td>
<td>2</td>
</tr>
<tr>
<td>3</td>
<td>0011</td>
<td>3</td>
<td>3</td>
</tr>
<tr>
<td>4</td>
<td>0100</td>
<td>4</td>
<td>4</td>
</tr>
<tr>
<td>5</td>
<td>0101</td>
<td>5</td>
<td>5</td>
</tr>
<tr>
<td>6</td>
<td>0110</td>
<td>6</td>
<td>6</td>
</tr>
<tr>
<td>7</td>
<td>0111</td>
<td>7</td>
<td>7</td>
</tr>
<tr>
<td>8</td>
<td>1000</td>
<td>10</td>
<td>8</td>
</tr>
<tr>
<td>9</td>
<td>1001</td>
<td>11</td>
<td>9</td>
</tr>
<tr>
<td>10</td>
<td>1010</td>
<td>12</td>
<td>A</td>
</tr>
<tr>
<td>11</td>
<td>1011</td>
<td>13</td>
<td>B</td>
</tr>
<tr>
<td>12</td>
<td>1100</td>
<td>14</td>
<td>C</td>
</tr>
<tr>
<td>13</td>
<td>1101</td>
<td>15</td>
<td>D</td>
</tr>
<tr>
<td>14</td>
<td>1110</td>
<td></td>
<td></td>
</tr>
<tr>
<td>15</td>
<td>1111</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
Q.1(d) Compare between synchronous and asynchronous counter (any two [2] points).

Ans.:

<table>
<thead>
<tr>
<th>Synchronous Counter</th>
<th>Asynchronous Counter</th>
</tr>
</thead>
<tbody>
<tr>
<td>1. All flip flops are triggered with same clock.</td>
<td>Different clock is applied to different flip flops.</td>
</tr>
<tr>
<td>2. It is faster.</td>
<td>It is lower</td>
</tr>
<tr>
<td>3. Design is complex.</td>
<td>Design is relatively easy.</td>
</tr>
<tr>
<td>4. Decoding errors not present.</td>
<td>Decoding errors present.</td>
</tr>
<tr>
<td>5. Any required sequence can be designed</td>
<td>Only fixed sequence can be designed.</td>
</tr>
</tbody>
</table>

Q.1(e) Draw the logical symbol of EX-OR and EX-NOR gate. [2]

Ans.:

EX-OR Gate:

EX-NOR Gate:

Q.1(f) Write simple examples of boolean expression for SOP and POS. [2]

Ans.:

SOP Form:

\[ Y = AB + BC + AC \]

POS Form:

\[ Y = (A + B)(B + C)(A + \bar{C}) \]

Q.1(g) Define modulus of a counter. Write the numbers of flip flops required for Mod-6 counter. [2]

Ans.:

- Modulus of counter is defined as number of states / clock the counter countes.
- The numbers of flip flops required for Mod-6 counter is 3.
Q.2 Attempt any Three of the following: [12]

Q.2(a) Minimize the following expression using K-Map. [4]
f(A,B,C,D) = \Sigma m(0, 1, 2, 4, 5, 7, 8, 9, 10)

Ans.: 

\[ Y = \overline{AC} + \overline{BC} + \overline{BD} + ABD \]

OR

\[ \overline{AC} + \overline{BC} + \overline{BD} + ABD \]

Q.2(b) Convert: \((AD92 \cdot BC A)_{16} = (?)_{10} = (?)_{8} = (?)_{2}\) [4]

Ans.: \((AD92.BCA)_{16}\)

\[ = (10 \times 16^3) + (13 \times 16^2) + (9 \times 16^1) + (2 \times 16^0) + (11 \times 16^{-1}) + (12 \times 16^{-2}) + (10 \times 16^{-3}) \]

\[ = 40960 + 3328 + 144 + 2 + 0.6857 + 0.046875 + 0.00244 \]

\[ = (44434.7368)_{10} \]

\((AD92.BCA)_{16} = (1010 11011001 0010.10111100 1010)_{2}\)

\((AD92.BCA)_{16} = (1010 11011001 0010.10111100 1010)_{2}\)

\[ = (001 010 110 110 010 010.101 111 001 010)_{2} \]

\[ = (126622.5712)_{8} \]

Note: any other method can be considered.

Q.2(c) Explain the following characteristics w.r.t logic families: [4]

(i) Noise margin  (ii) Power dissipation
(iii) Figure of merit  (iv) Speed of operation
Ans.: (i) **Noise margin**: Noise margin indicates the amount to noise voltage circuit can tolerate at its input for both logic 1 and logic 0.
(ii) **Power dissipation**: It is the amount of power dissipated in an IC.
(iii) **Figure of merit**: It is defined as the product of propagation delay and power dissipated by the gate.
(iv) **Speed of operation**: Speed of logic circuit is determined by the time between the application of input and change in the output of the circuit.

**Q.2(d) Draw and explain PAL.**

**Ans.**: The PAL represents another alternative to PROMs. This device was introduced by monolithic memories. The PAL suffers from the PROM in that the input AND gate connections are programmable in PAL, whereas the output OR gate connectors are programmable in PROM.

![Example of PAL](image-url)
Q.3 Attempt any Three of the following:  

Q.3(a) Draw the circuit diagram and draw waveform for ring counter.  

Ans.:  

Basically ring counter resembles shift register because the bits are shifted left one position per positive clock edge. Only change is feedback line i.e. output of Q3 given to Q0.

Q.3(b) Draw the circuit of successive approximation type ADC and explain it's working.  

Ans.:
The successive approximation A/D converter is as shown in fig. An analog voltage (Va) is constantly compared with voltage Vi, using a comparator. The output produced by comparator (Vo) is applied to an electronic Programmer. If Va=Vi, then Vo = 0 & then no conversion is required. The programmer displays the value of Vi in the form of digital O/P.

But if Va Vi, then the O/P is changed by the programmer.
If Va > Vi, then value of Vi is increased by 50% of earlier value.
But if Va < Vi, then value of Vi is decreased by 50% of earlier value.

This new value is converted into analog form, by D/A converter so as to compare it with Va again. This procedure is repeated till we get Va = Vi. As the value of Vi is changed successively, this method is called as successive-approximation A/D converter.

Q.3(c) Describe the function of Full Adder Circuit using its truth table, K-Map simplification and logic diagram.

Ans.: A full adder is a combinational logic circuit that performs addition between three bits, the two input bits A and B and carry C from the previous bit.

Block diagram:

![Block Diagram of Full Adder](image)

Truth Table:

<table>
<thead>
<tr>
<th>Input</th>
<th>Output</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>B</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>
Q.3(d) Realize the basic logic gates, NOT, OR and AND gates using NOR [4] gates only.

Ans.:

where, \( X = A \text{ NOR } A \)
\[
x = \overline{A}
\]

\[
Q = \overline{A + B} = \overline{A} + \overline{B}
\]
\[
= A \cdot B
\]

\[
Q = A + B = A + B
\]
Q.4 Attempt any Three of the following: [12]

Q.4(a) Subtract the given number using 2’s complement method: [4]

(i) \((11011)_2 - (11100)_2\)
(ii) \((1010)_2 - (101)_2\)

Ans.: (i) \((11011)_2 - (11100)_2\)

Now,
2’s complement of \((11100)_2\) = 1’s complement of \((11100)_2\) + 1
1’s complement of \((11100)_2\) = \((00011)_2\)
2’s complement = \(00011 + 1 = 00100\)
Therefore,

\[
\begin{array}{c}
1 \\
+ \\
\hline
1 1 0 1 1
\end{array}
\]

\[
\begin{array}{c}
0 0 1 0 0
\end{array}
\]

\[
\begin{array}{c}
1 1 1 1 1
\end{array}
\]

There is no carry it indicates that results is negative and in 2’s complement form i.e.\((11111)_2\).
Therefore, for getting true value i.e.(+1) take 2’s complement of \((11111)_2\) is 1’s complement + 1
\[
= 00000 + 1
= (00001)_2
\]

\((11011)_2 - (11100)_2 = 2’s\ complement\ of\ (11111)_2 = (-1)_{10}\)

(ii) Subtract \((1010)_2 - (101)_2\) using 2’s complement binary arithmetic.

2’s complement of \((0101)_2 = 1’s\ complement\ of\ (0101)_2 + 1\)
1’s complement of \((0101)_2 = (1010)_2\)
2’s complement = \(1010 + 1 = 1011\)
Therefore,

\[
\begin{array}{c}
1 0 1 0
\end{array}
\]

\[
\begin{array}{c}
1 0 1 1
\end{array}
\]

\[
\begin{array}{c}
1
\end{array}
\]

\[
\begin{array}{c}
1 0 1 0 1
\end{array}
\]

There is carry ignore it, which indicates that results is positive i.e.(+5)
\[
= (0101)_2
\]

\((1010)_2 - (101)_2 = (0101)_2 = (+5)_{10}\)
Q.4(b) State De-Morgan’s theorem and prove any one. [4]
Ans.: It states that the compliment of sum is equal to the product of the compliment of individual variables.
\[(\overline{A + B}) = \overline{A} \overline{B}\]
Proof:
\[
\begin{array}{|c|c|c|c|c|c|}
\hline
A & B & \overline{A} & \overline{B} & A + B & (\overline{A + B}) & \overline{A} \overline{B} \\
\hline
0 & 0 & 1 & 1 & 0 & 1 & 1 \\
0 & 1 & 1 & 0 & 1 & 0 & 0 \\
1 & 0 & 0 & 1 & 1 & 0 & 0 \\
1 & 1 & 0 & 0 & 1 & 0 & 0 \\
\hline
\end{array}
\]

De Morgan’s 2nd Theorem:
It states that the compliment of product is equal to the sum of the compliments of individual variables.
\[(\overline{A B}) = \overline{A} + \overline{B}\]
Proof:
\[
\begin{array}{|c|c|c|c|c|c|}
\hline
A & B & \overline{A} & \overline{B} & A . B & (\overline{A B}) & \overline{A} + \overline{B} \\
\hline
0 & 0 & 1 & 1 & 0 & 1 & 1 \\
0 & 1 & 1 & 0 & 0 & 1 & 1 \\
1 & 0 & 0 & 1 & 0 & 1 & 1 \\
1 & 1 & 0 & 0 & 1 & 0 & 0 \\
\hline
\end{array}
\]

Q.4(c) Design 16:1 mux using 4:1 mux. [4]
Ans.:

Ans.:

Explanation
If a logic “1” is connected to the DATA input pin of FFA then on the first clock pulse the output of FFA and therefore the resulting QA will be set HIGH to logic “1” with all the other outputs still remaining LOW at logic “0”.

Assume now that the DATA input pin of FFA has returned LOW again to logic “0” giving us one data pulse or 0-1-0.

The second clock pulse will change the output of FFA to logic “0” and the output of FFB and QB HIGH to logic “1” as its input D has the logic “1” level on it from QA. The logic “1” has now moved or been “shifted” one place along the register to the right as it is now at QA.

When the third clock pulse arrives this logic “1” value moves to the output of FFC (QC) and so on until the arrival of the fifth clock pulse which sets all the outputs QA to QD back again to logic level “0” because the input to FFA has remained constant at logic level “0”.

The effect of each clock pulse is to shift the data contents of each stage one place to the right, and this is shown in the following table until the complete data value of 0-0-0-1 is stored in the register. This data value can now be read directly from the outputs of QA to QD.

Then the data has been converted from a serial data input signal to a parallel data output. The truth table and following waveforms show the propagation of the logic “1” through the register from left to right as follows.
Basic Data Movement Through A Shift Register

<table>
<thead>
<tr>
<th>Clock Pulse No</th>
<th>QA</th>
<th>QB</th>
<th>QC</th>
<th>QD</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>2</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>3</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>4</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>5</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

Q.4(e) Calculate analog output of 4 bit DAC for digital input 1101. [4]

Assume $V_{FS} = 5V$.

Ans.:

$$V_0 = V_R \left[ d_3 2^{-1} + d_2 2^{-2} + ... + d_n 2^{-n} \right]$$

$$= 5(1 \times 2^{-1} + 1 \times 2^{-2} + 0 \times 2^{-3} + 1 \times 2^{-4})$$

$$= 5(0.5 + 0.25 + 0 + 0.0625)$$

$$= 4.0625 \text{ volts}$$

OR

$$V_{FS} = V_R \left( \frac{b_3}{2} + \frac{b_2}{4} + \frac{b_1}{8} + \frac{b_0}{16} \right)$$

Note – (Since $V_R$ is not given find $V_R$)

Full Scale o/p mean

$b_3 b_2 b_1 b_0 = 1111$

$V_{FS} = 5V$

$$5 = V_R \left( \frac{1}{2} + \frac{1}{4} + \frac{1}{8} + \frac{1}{16} \right)$$

$V_R = 5.33$

For digital input $b_2 b_1 b_0 = 1101$

$$V_0 = 5.33 \left( \frac{1}{2} + \frac{1}{4} + \frac{0}{8} + \frac{1}{16} \right)$$

$$V_0 = 4.33 \text{ V}$$
Q.5 Attempt any TWO of the following:
Q.5(a) Design a 4 bit synchronous counter and draw its logic diagram.
Ans.: State Table

<table>
<thead>
<tr>
<th>Present state</th>
<th>Next state</th>
<th>Flip flop inputs</th>
</tr>
</thead>
<tbody>
<tr>
<td>D  C  B  A</td>
<td>D'  C'  B'  A'</td>
<td>T_D  T_C  T_B  T_A</td>
</tr>
<tr>
<td>0  0  0  0</td>
<td>0  0  0  1</td>
<td>0  0  0  1</td>
</tr>
<tr>
<td>0  0  0  1</td>
<td>0  0  1  0</td>
<td>0  0  1  1</td>
</tr>
<tr>
<td>0  0  1  0</td>
<td>0  0  1  1</td>
<td>0  0  0  1</td>
</tr>
<tr>
<td>0  0  1  1</td>
<td>0  1  0  0</td>
<td>0  1  1  1</td>
</tr>
<tr>
<td>0  0  1  1</td>
<td>0  1  1  1</td>
<td>0  0  0  1</td>
</tr>
<tr>
<td>0  1  0  0</td>
<td>0  1  0  1</td>
<td>0  0  1  1</td>
</tr>
<tr>
<td>0  1  0  1</td>
<td>0  1  1  0</td>
<td>0  0  1  1</td>
</tr>
<tr>
<td>0  1  1  0</td>
<td>0  1  1  1</td>
<td>0  0  0  1</td>
</tr>
<tr>
<td>0  1  1  1</td>
<td>1  0  0  0</td>
<td>1  1  1  1</td>
</tr>
<tr>
<td>0  1  1  1</td>
<td>1  0  0  1</td>
<td>0  0  0  1</td>
</tr>
<tr>
<td>1  0  0  0</td>
<td>1  0  1  0</td>
<td>0  0  1  1</td>
</tr>
<tr>
<td>1  0  0  1</td>
<td>1  0  1  1</td>
<td>0  0  0  1</td>
</tr>
<tr>
<td>1  0  1  0</td>
<td>1  1  0  0</td>
<td>0  1  1  1</td>
</tr>
<tr>
<td>1  0  1  1</td>
<td>1  1  0  1</td>
<td>0  0  0  1</td>
</tr>
<tr>
<td>1  1  0  0</td>
<td>1  1  1  0</td>
<td>0  0  1  1</td>
</tr>
<tr>
<td>1  1  0  1</td>
<td>1  1  1  1</td>
<td>0  0  0  1</td>
</tr>
<tr>
<td>1  1  1  0</td>
<td>0  0  0  0</td>
<td>1  1  1  1</td>
</tr>
</tbody>
</table>

K-maps for T_D, T_C, T_B, T_A
Q.5(b) Design mod-3 Asynchronous counter and draw output waveform. [6]

Ans.: Design mod – 3 Asynchronous counter and draw output waveform.

To design mod-3 counter we required 2 flip-flops

<table>
<thead>
<tr>
<th>( Q_B )</th>
<th>( Q_A )</th>
<th>( y(output) )</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
</tbody>
</table>

Design a reset logic combinational circuit such that output \( y \) should be 1 when valid states are there and \( y = 0 \) when invalid states are present.

\[
y = \overline{A} + \overline{B} = AB
\]

Logic Diagram :
Q.5(c) Design BCD to seven segment decoder using IC 7447 with its truth table.

Ans.: Note: Any one type of display shall be considered

1. BCD to 7 segment decoder is a combinational circuit that accepts 4 bit BCD input and generates appropriate 7 segment output.
2. In order to produce the required numbers from 0 to 9 on the display the correct combination of LED segments need to be illuminated.
3. A standard 7 segment LED display generally has 8 input connections, one from each LED segment & one that acts as a common terminal or connection for all the internal segments.
4. Therefore there are 2 types of display 1. Common Anode Display 2. Common Cathode

Display:
Common Anode Display

![Diagram of BCD to 7 segment decoder using IC 7447]

Truth Table

<table>
<thead>
<tr>
<th>BCD Input (ABC)</th>
<th>7 Segment Coded Output (abcdefg)</th>
<th>Display Outputs</th>
</tr>
</thead>
<tbody>
<tr>
<td>000</td>
<td>00000000</td>
<td>0</td>
</tr>
<tr>
<td>000</td>
<td>00000001</td>
<td>1</td>
</tr>
<tr>
<td>...</td>
<td>...</td>
<td>...</td>
</tr>
<tr>
<td>101</td>
<td>00000001</td>
<td>1</td>
</tr>
<tr>
<td>111</td>
<td>00000000</td>
<td>0</td>
</tr>
</tbody>
</table>

For normal functioning, R1, R2, R3, R4 should be connected to logic 1.
Q. 6 Attempt any TWO of the following: [12]

Q. 6(a) Design 4 bit Binary to Gray code converter. [6]

Ans.: Truth table for 4 bit Binary to Gray code converter.

<table>
<thead>
<tr>
<th>Binary Input</th>
<th>Gray output</th>
</tr>
</thead>
<tbody>
<tr>
<td>B3</td>
<td>B2</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
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<tr>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
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<tr>
<td>1</td>
<td>1</td>
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<tr>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

K - MAP for G3:

\[ G3 = B3 \]
K-MAP For G2:
\[ G2 = \overline{B3} B2 + B2 B3 = B3 \oplus B2 \]

K-MAP For G1:
\[ G1 = \overline{B2} B1 + B2 \overline{B1} = B1 \oplus B2 \]

K-MAP FOR G0:
\[ G0 = B1B0 + B1\overline{B0} = B1 \oplus B0 \]

Diagram for 4 bit Binary to Gray code converter:

Note: Realization of output equations can be done using Basic or Universal gates.
Q.6(b) How can IC 7490 can used as a decade counter with neat block [6] diagram.

Ans.: Explanation

IC 7490: It consists of two counters namely MOD 2 and MOD 5. Thus IC 7490 can be used as MOD 2 or MOD 5 counter independently. When this IC need to be used as MOD 10 i.e. decade counter, the o/p of MOD 2 counter i.e. QA need to be connected to the clock i/p of MOD 5 counter as shown below thus acting as a 4 bit MOD 10 counter.

![Truth Table](image)

Fig.: IC 7490 be used as a decade counter
Q.6(c) Draw the circuit diagram of 4 bit R-2R ladder DAC and obtain its output voltage expression.

Ans.:

Fig. 1: 4 bit R-2R ladder DAC

Fig. 2: Simplified circuit diagram of Fig. 1

Therefore output analog voltage \( V_0 \) is given by,

\[
V_0 = \left( \frac{RF}{3R} \right) \left( \frac{VR}{2^4} \right) b_0 + \left( \frac{RF}{3R} \right) \frac{VR}{2^3} b_1 + \left( \frac{RF}{3R} \right) \frac{VR}{2^2} b_2 + \left( \frac{RF}{3R} \right) \frac{VR}{2^1} b_3
\]

\[
V_0 = -\left( \frac{RF}{3R} \right) \left( \frac{VR}{2^4H4} \right) \left[ 8b_3 + 4b_2 + 2b_1 + b_0 \right]
\]